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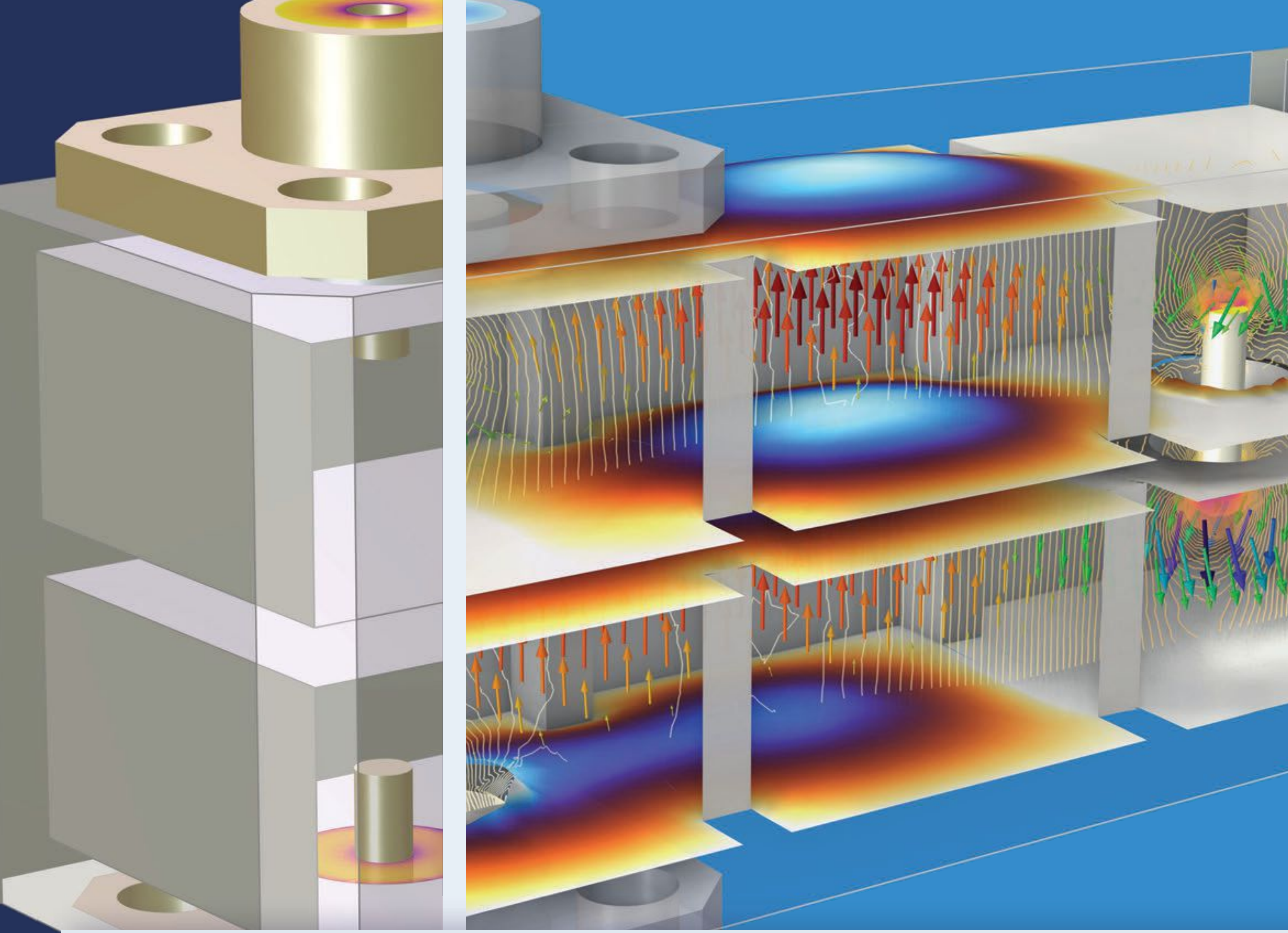

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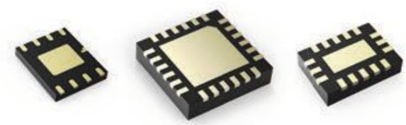

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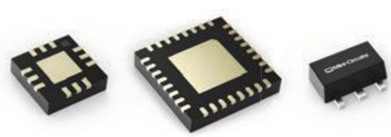

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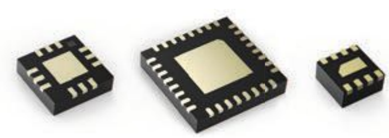

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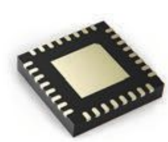

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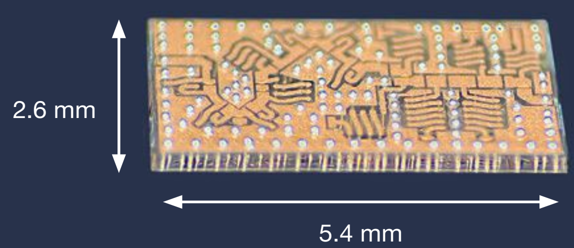

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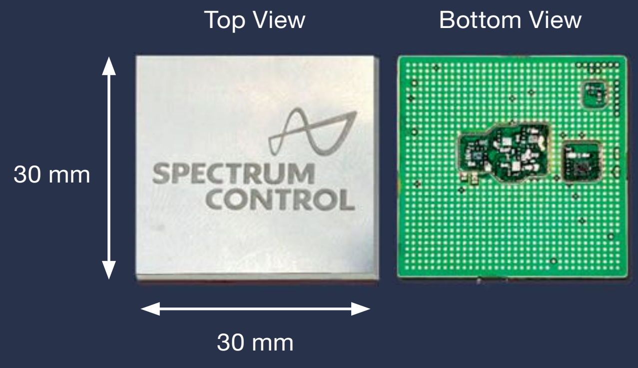

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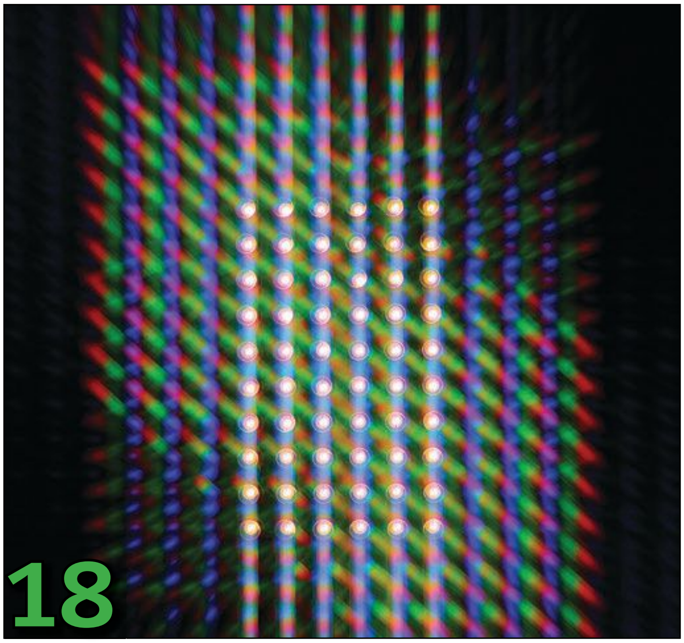

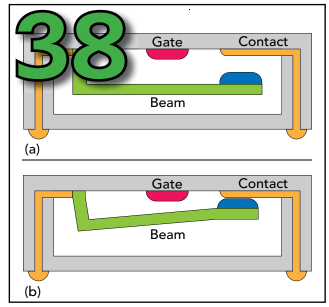

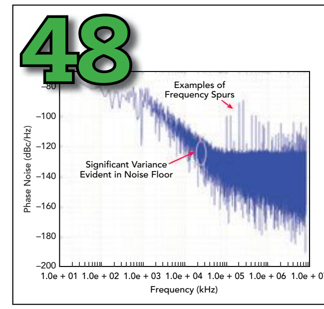

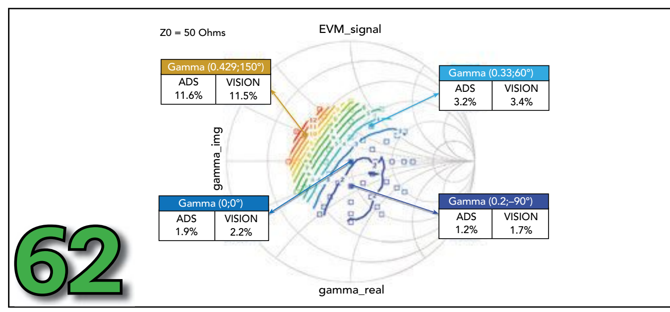

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Application Note

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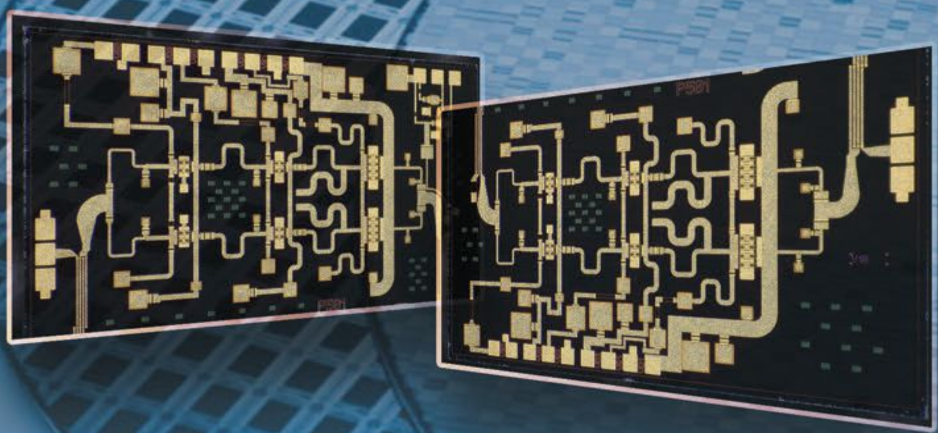

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RF Distributed Low Noise Amplifiers

PN	Freq Low (GHz)	Freq High (GHz)	Gain (dB)	NF(dB)	P1dB (dBm)	Voltage (VDC)	Current (mA)	Package
MMW001T	DC	20.0	17~19	1~3.5	23 @ 10GHz	8.0	145	die
MMW4FP	DC	50.00	16.00	4.00	24.00	10	200	die
MMW507	0.20	22.0	14.0	4 - 6	28.0	10.0	350	die
MMW508	DC	30.0	14.0	2.5dB @ 15GHz	24.5	10.0	200	die
MMW509	30KHz	45.0	15.0		20.0	6.0	190	die
MMW510	DC	45.0	11.0	4.5	15.5	6.0	100	die
MMW510F	DC	30.00	20.00	2.50	22.00			die
MMW511	0.04	65.0	10.0	9.0	18.0	8.0	250	die
MMW512	DC	65.0	10.0	5.0	14.5	4.5	85	die
MMW5FN	DC	67.00	14.00	2.00	19.00	4.5	81	die
MMW5FP	DC	67.00	14.00	4.00	21.00	8	140	die
MMW011	DC	12.0	14.0		30.5	12.0	350	die

Low Noise Amplifiers

PN	Freq Low (GHz)	Freq High (GHz)	Gain (dB)	NF(dB)	P1dB (dBm)	Voltage (VDC)	Current (mA)	Package
MML040	6.0	18.0	24.0	1.5	14.0	5.0	35	die
MML058	1.0	18.0	15.0	1.7	17.0	5.0	35	die
MML063	18.0	40.0	11.0	2.9	15.0	5.0	52	die
MML080	0.8	18.0	16.5/15.5	1.9/1.7	18/17.5	5.0	65/40	die
MML081	2.0	18.0	25/23	1.0/1.0	16/9.5	5.0	37/24	die
MML083	0.1	20.0	23.0	1.6	11.0	5.0	58	die

RF Driver Amplifier

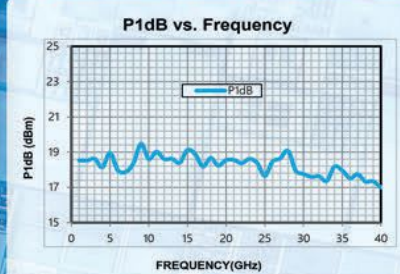
PN	Freq Low (GHz)	Freq High (GHz)	Gain (dB)	NF(dB)	P1dB (dBm)	Voltage (VDC)	Current (mA)	Package
MM3006	2.0	20.0	19.5	2.5	22.0	7.0	130	die
MM3014	6.0	20.0	15.0	-	19.5	5.0	107	die
MM3017T	17.0	43.0	25.0		22.0	5.0	140	die
MM3031T	20.0	43.0	20.0		24.0	5.0	480	die
MM3051	17.0	24.0	25.0	-	25.0	5.0	220	die
MM3058	18.0	40.0	20/19.5	2.5/2.3	16/14	5/4	69/52	die
MM3059	18.0	40.0	16/16	2.5/2.3	16/15	5/4	67/50	die

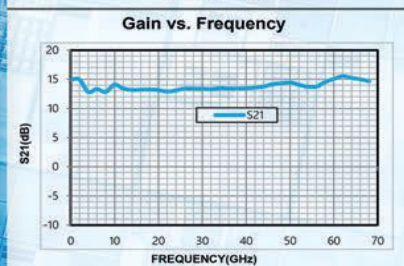
GaAs Medium Power Amplifier

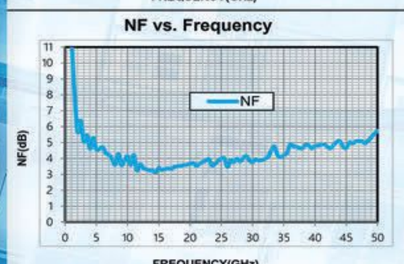
PN	Freq Low (GHz)	Freq High (GHz)	Gain (dB)	P1dB (dBm)	Psat (dBm)	Voltage (VDC)	Current (mA)	Package
MMP107	17.0	21.0	19.0	30.0	30.0	6.0	400	die
MMP108	18.0	28.0	14.0	31.5	31.0	6.0	650	die
MMP111	26.0	34.0	25.5	33.5	33.5	6.0	1300	die
MMP112	2.0	6.0	20.0	31.5	32.0	8.0	365	die
MMP501	20.0	44.0	15.0	27 -- 32	29 - 34	5.0	1200	die
MMP502	18.0	47.0	14.0	28.0	30.0	5.0	1500	die

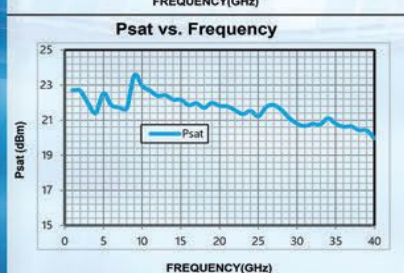
PN: MMW5FP

RF GaAs MMIC DC-67GHz









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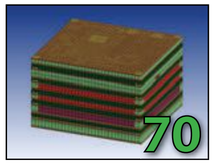

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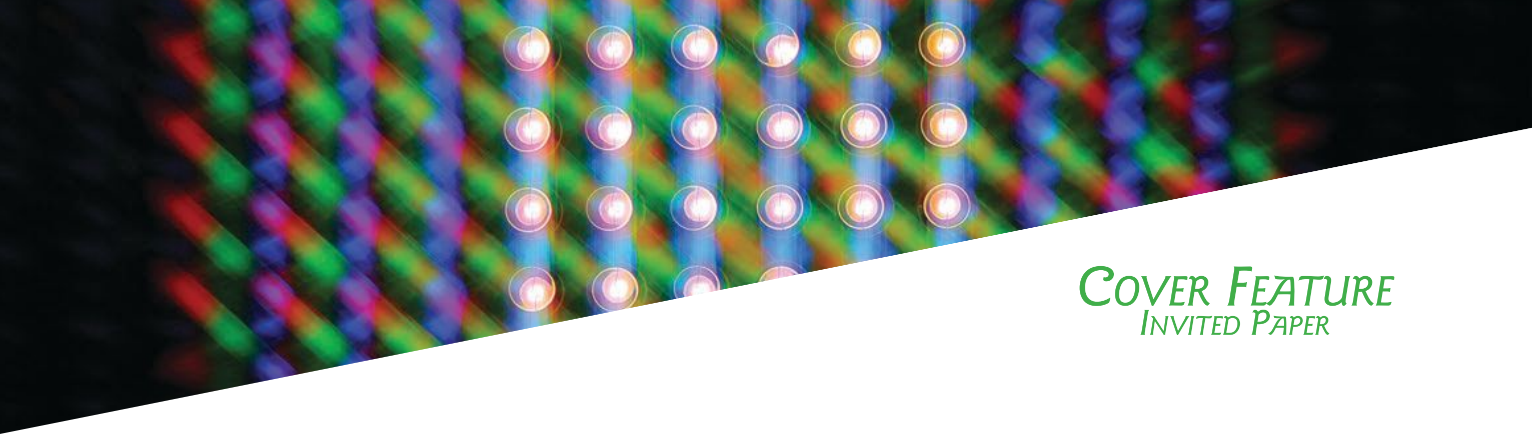

Cover Feature
Invited Paper

Efficiently Simulating Phased Arrays With Active Impedance

Murthy Upmaka and Eva Ribes-Vilanova
Keysight Technologies, Santa Rosa, Calif.

Don Dingee
STRATISET, San Antonio, Texas

Phased arrays, more formally known as active electronically steerable arrays (AESAs), are a popular architectural choice for radar, 5G and 6G base stations, satellite communication platforms and mobile device applications. When optimized, beamforming via phased arrays improves signal quality, data throughput and user experience. As array sizes grow, so does the difficulty in designing and optimizing antenna elements and signal processing. Physical evaluation in anechoic chambers can take weeks and setups striving to represent real-world conditions may be incomplete, tenuous or infeasible. The alternative is simulating phased array designs quickly, inexpensively and accurately reproducing behaviors and effects in virtual space.

System-level simulations with measurement-based models, authentic modulation at full bandwidth, circuit and electromagnetic (EM) co-simulation, cross-domain analysis and other techniques can reproduce complex scenarios accurately and inform design optimizations. However, high-fidelity simulation comes with computational costs and with phased arrays scaling into the hundreds and soon, thousands of elements, simulation time becomes a concern. Adding to the phased array analysis complexity are effects associated with array active impedance, where elements couple and interact under array excitation.

Array active impedance is receiving increased attention from electronic design automation (EDA) researchers at Keysight. Teams approach real-world problems in three phases: developing models via measurements or simulations, testing the accuracy of those models in simulations with real-world conditions and then generalizing models and simulations to evaluate more complex applications at scale.

Phased array design is an example of how this approach to EDA research pays off. A behavioral simulation methodology using Keysight SystemVue decomposes large phased arrays with their signal processing chains into smaller tiles for S-parameter coupling matrix extraction, then stitches tiles together with element remapping to represent the entire array with active impedance effects in fast, accurate virtual analysis. This article will explore this more efficient methodology in four parts, including a first look at a patented technique for building the required full-array S-parameter matrix from a smaller matrix:

- Accurate array behavioral modeling from measured or EM-simulated embedded element patterns
- High-fidelity modeling of power amplifiers (PAs) under load-pull conditions
- Iteratively capturing array active impedance with beamforming applied
- Extending far-field pattern simulations from smaller to larger phased array systems.

ACCURATE ARRAY BEHAVIORAL MODELING FROM MEASURED OR EM-SIMULATED EMBEDDED ELEMENT PATTERNS

Traditionally, designers measured antenna elements to understand patterns. Advances in circuit/EM co-simulation techniques using ADS in the workflow provide a faster, less expensive way to predict phased array element behavior before fabricating physical devices. ***Figure 1*** shows a layout of a 4 × 8 array in ADS for EM simulation with Keysight RFPro.

RFPro simulation produces an embedded element pattern in a .ffio file by automatically exciting the entire array one element at a time with all other element ports terminated, capturing the pattern of every element in its position in the array. Element patterns differ depending on metallization, structural details and position of the element in the array. Elements also exhibit EM coupling, where energy radiated from one element is picked up by others. Modeling this mutual coupling is essential to accurately predicting far-field patterns of an array. The simulation also produces an S-parameter matrix representing the entire array.

A SystemVue model of an array starts with an antenna configuration preserving the exact mapping of numbered element locations corresponding to the ADS layout. Then, the embedded element pattern and the S-parameter matrix are imported. ***Figure 2*** shows a simple schematic for the 4 × 8 array and import dialogs to complete the configuration.

Moving from a detailed EM simulation to a behavioral simulation loses little to no fidelity, as shown in the boresight pattern plots in ***Figure 3***. However, the computational reduction is significant. EM simulation of the whole array is feasible for small arrays. However, as element counts increase toward 100 and beyond, effect complexity increases and the advantage of reduced behavioral simulation time becomes apparent, becoming even more so with simplifications to array models discussed shortly.

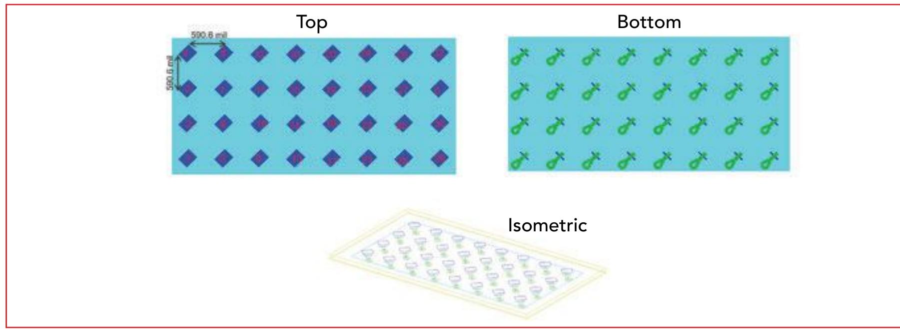

Fig. 1 Antenna array layout in ADS.

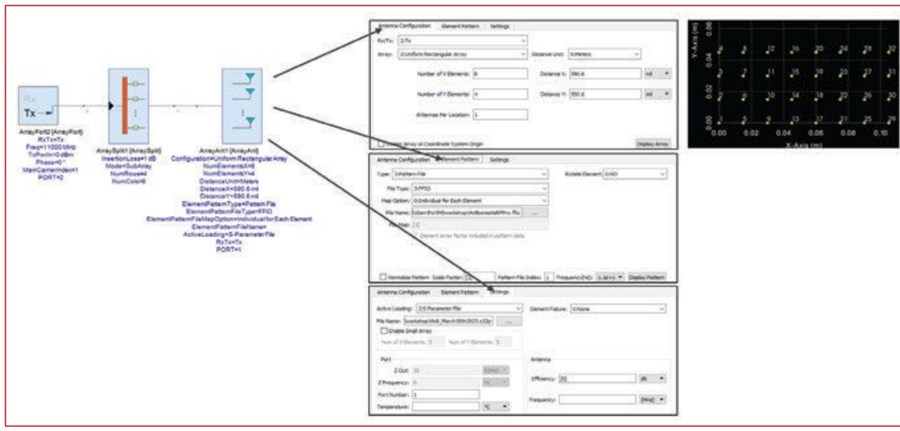

Fig. 2 Importing the element pattern and S-parameter matrix from the SystemVue schematic.

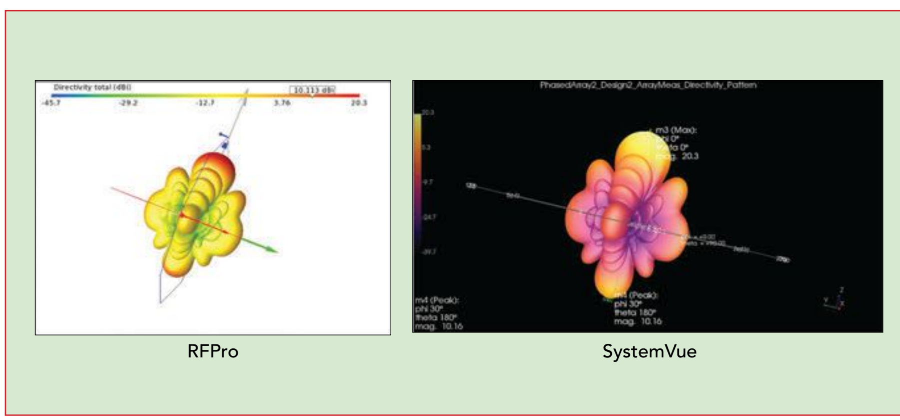

Fig. 3 Boresight pattern plots from EM (RFPro) and behavioral (SystemVue) simulations.

HIGH-FIDELITY MODELING OF PAS UNDER LOAD-PULL CONDITIONS

RF PA design is an excellent example of how multi-variable optimization becomes necessary. Designers look at gain, peak and average power delivery and efficiency, distortion, linearity, noise and other performance metrics across a given bandwidth. Changing any feature of a PA typically affects several metrics. Circuit/EM co-simulations can sweep a set of parameters simultaneously and optimization techniques can explore a multi-dimensional surface and look for the best results.

Load-pull analysis provides deeper insight into PA performance when drive impedance, the load the amplifier sees, varies. Low frequency PAs usually define a fixed resistive termination as the load, such as 50 or 75 Ω, creating an operating point for optimization. Changing drive impedance pulls the PA away from its intended operating point, often unpredictably, with cross-domain interactions.

Figure 4 shows a load-pull analysis for a simple one-amplifier schematic in ADS. Harmonic balance simulation uses a single tone plus harmonics with swept input power and different load impedances at harmonic frequencies. The simulation exposes PA distortion and non-linearity while capturing gain, output power and power-added efficiency at each load impedance. Also plotted in Figure 4 is a Smith chart with a contour indicating shifts in the PA's S-parameters as the load changes.

In a phased array design, loads on PAs in each element's signal processing chain change continuously due to the effects of array active impedance. This makes the behavioral characterization of a PA with load-pull effects incorporated imperative. Load-pull analysis with circuit/EM simulation in ADS results in changes to the PA's X-parameter matrix describing its behavior.

Importing the load-pull enabled PA X-parameter matrix into SystemVue provides a high-fidelity PA model for more accurate behavioral simulation. Each element in the phased array has a complete RF signal processing chain with PAs and other components such as phase shifters. With insight from a load-pull analysis, one optimized chain needs replication for the number of elements in the array. Smart models help condense a set of these chains into a single line. ***Figure 5*** shows the behavioral model for an 8 × 8 phased array.

Following the methodology described so far, this simplified phased array behavioral model now contains antenna patterns for each element. It also includes basic EM coupling effects between elements and load-pull effects on the PAs behind each element. While this adds significant fidelity to the model, two more steps are needed to accurately capture real-world phased array behavior.

ITERATIVELY CAPTURING ARRAY ACTIVE IMPEDANCE WITH BEAMFORMING APPLIED

Phased arrays have one fundamental purpose: beamforming. This is the process of steering and shaping a beam for its context. In radar systems, a wide beam offers faster detection, with narrower beams used to track one or more targets after acquisition. In 5G and 6G systems, beamforming at the base station and mobile device creates massive MIMO connections for optimum data throughput. Satellite systems apply beamforming to improve link margin and overcome channel interference.

Beamforming uses a phased array or one or more subsets of its elements to create beams with specific directions and shapes. In addition to the raw EM coupling between elements due to layout and structural issues, the weight, steering angle and phase shift of a beam applied to the array or a subarray results in each element presenting active impedance. Two time-varying effects ensue: a load-pull effect on the PAs with mutual coupling effects across elements. These simultaneous effects, more complex than found in the separate analyses of the elements and PAs, alter the intended shape of a beam.

After developing detailed models with frequency-domain simulations, fully uncovering array active impedance effects on far-field patterns requires time-domain simulation with representative beamforming stimuli. ***Figure 6*** shows the XParam model in the data flow used to simulate phased array systems containing amplifiers described with X-parameters files with load-pull information and to model antenna active impedance.

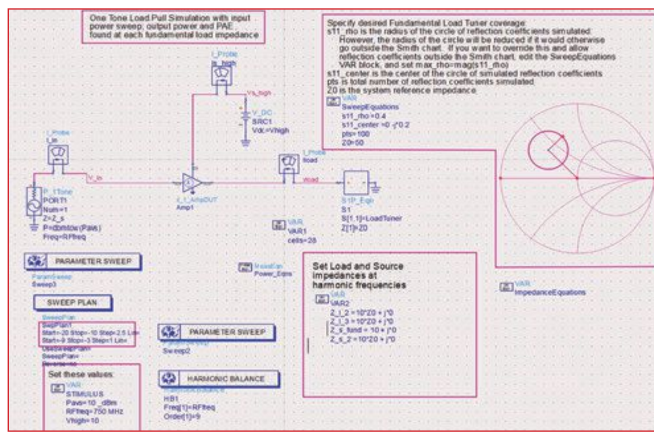

Fig. 4 Load-pull analysis for a PA using a harmonic balance simulation in ADS.

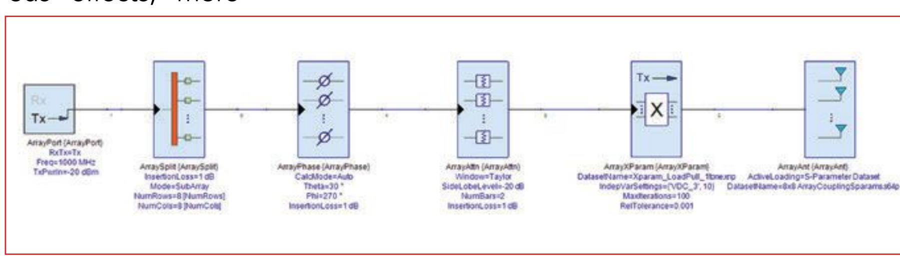

Fig. 5 Architectural view of an RF signal processing chain in SystemVue.

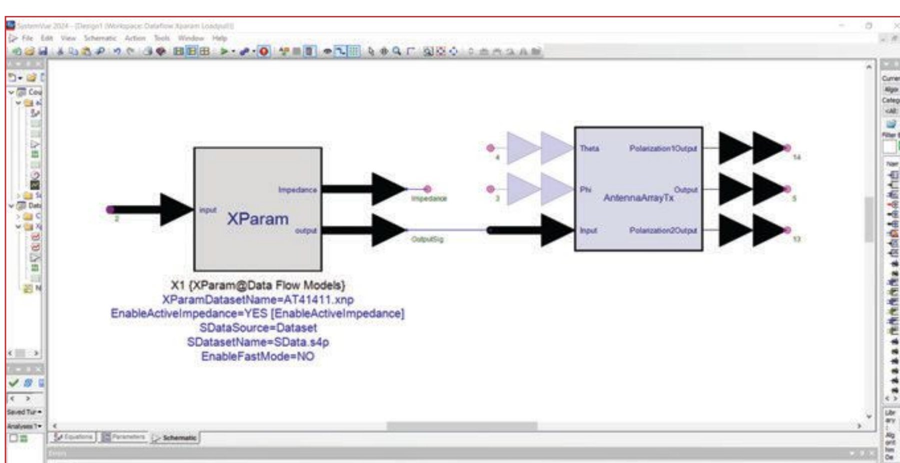

Fig. 6 Adding array active impedance with an XParam model in the time-domain data flow simulation.

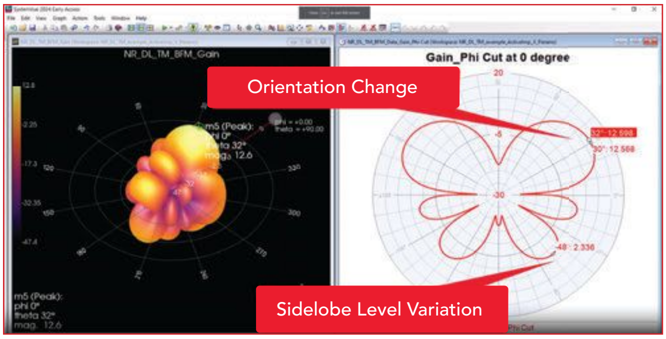

Fig. 7 5G NR beam orientation change with array active impedance enabled.

First, the time-domain simulation generates a beam steered at a 30-degree angle with only an imported X-parameter model for PA load-pull. For the next step, the simulation imports the antenna element patterns and the element coupling matrix and enables active impedance. ***Figure 7*** shows a phi cut plot indicating a two-degree shift in the beam angle and significant sidelobe level variation with active impedance enabled.

Simulation users see only a "yes/no" switch to enable active impedance in the analysis. Behind the scenes in SystemVue are calculations using X-parameter representations of the PAs and the coupling matrix of the antenna elements. The challenge is that PA load impedance values depend on knowing the reflection coefficients of the antenna ports. These values are unknown initially, preventing sequential calculation. Simulations work iteratively to converge incident and scattered voltage waves into and out of the PAs and the element reflection coefficients. Then, the time-domain data flow simulation calculates the actual impedance seen by each of the PAs, including the coupling effect between elements. Also, enhancements to data storage streamline the iterative calculations searching for PA operating points, avoiding repeated passes where amplitude and phase values are the same as in prior passes.

Time-domain analysis innovations position phased array designers to have more accurate insight into system-level performance, especially far-field patterns, than previously possible with only frequency-domain analysis. Still, as array sizes grow, S-parameter matrices expand, driving simulation times exponentially higher. A simplification of the array representation reins in simulation complexity while retaining behavioral model fidelity.

EXTENDING FAR-FIELD PATTERN SIMULATIONS FROM SMALLER TO LARGER ARRAYS

Keysight researchers observed that circuit/EM co-simulation time starts becoming uncomfortably long at around 100 unique elements, such as in a 10 × 10 array. This raised the question of whether building larger arrays from smaller ones would be possible in virtual space, avoiding long simulation times by leveraging detailed analysis of fewer elements and signal chains and accurately extending those behaviors to other elements in the model. U.S. Patent

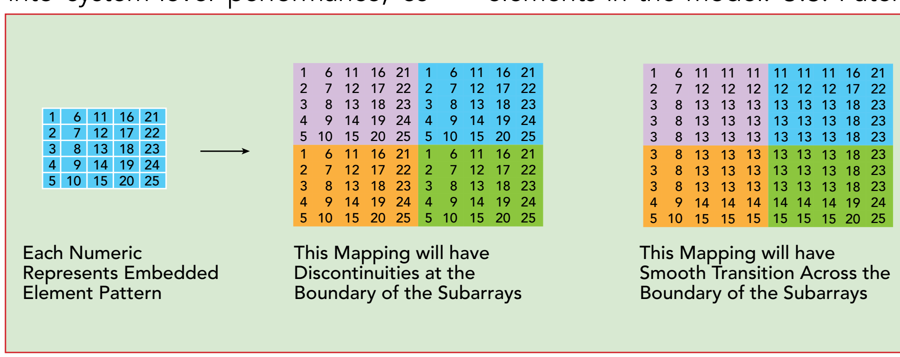

Fig. 8 Remapping 25 elements from a 5 x 5 array into a 10 x 10 array.

11,921,144 describes such a method directly applicable to system-level behavioral simulations.

The idea of scaling from smaller arrays begs the question: are all individual element behaviors in larger arrays unique? Empirical analysis shows that each element displays significant EM coupling with adjacent elements and some coupling with elements two places away in any direction. After a two-element distance, coupling diminishes to insignificance. The two-element coupling distance observation suggests the minimum array size for detailed active impedance analysis should be 5 × 5, where the coupling of each element is unique. A 5 × 5 array is convenient for illustration purposes, but other odd array sizes, such as 7 × 7 or 9 × 9, work with the method about to be described.

Figure 8 begins on the left with a 5 × 5 subarray and 25 uniquely-numbered elements. Element 13 is coupled to every other element since all are within a two-element distance, while Element 1 couples to only eight as a boundary condition. A naïve assumption would tile 5 × 5 subarrays to reach bigger uniform rectangular array sizes. However, with EM coupling between elements considered, simple tiling creates discontinuities, violating coupling behavior at the subarray boundaries. Element 1 in the upper right subarray in the middle of Figure 8, as analyzed in the 5 × 5 subarray, does not expect to couple with elements to its left, with the same being true for Element 21 in the upper left subarray looking to its right.

Boundary conditions need addressing if tiles are to scale without repeating detailed analysis. Moving into a 10 × 10 array, remapping array elements starting from their positions in the 5 × 5 subarray solves the edge discontinuities. Each element is no longer unique and coupling in the full 10 × 10 array is accurately represented using only the 25 elements from the 5 × 5 array. Element 13 repeats in the remapped 10 × 10 array on the right of Figure 8, where the two-element coupling distance in any direction applies. Similarly, other elements repeat with their coupling relationships in the 5 × 5 subarray preserved.

Exhaustive analysis of the 5 × 5 subarray with load-pull and EM coupling recognized results in accurate S-parameter properties for each of its 25 elements. Simplifying the 10 × 10 array with 75 percent fewer unique elements by mapping their associated S-parameter properties into a larger S-parameter matrix provides significant gains in simulation time and the savings grow with even bigger arrays. The method also preserves fidelity; simulations of 10 × 10 arrays with simplified remapped elements agree to four decimal places with simulations of 10 × 10 arrays using 100 unique elements. Generalizing the technique allows designers to model phased arrays of hundreds or even thousands of elements.

ENABLING ITERATIVE PHASED ARRAY DESIGN IN ONE VIRTUAL WORKFLOW

Phased array designers may have had a qualitative understanding of array active impedance but not an effective way to quantify it without lengthy trial-and-error cycles of measurements, design adjustments and hardware re-spins. Fortunately, behavioral simulation technology and modeling advancements have caught up. They provide a shift left to accurate results in virtual space earlier in the phased array design cycle.

Simplifying system-level behavioral modeling for efficient simulation of phased arrays is a significant breakthrough. The crucial addition of time-domain data flow simulation capability and the insight into remapping elements enables designers to spend more time calibrating and optimizing the design of the array elements and RF signal processing chains. These techniques also allow quick iterations of simulations to confirm results, even as phased array sizes scale much larger. ■

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Cliff Drubin, Associate Technical Editor

Cutting-Edge Drone Killer Radio Wave Weapon Developing at Pace

A new game-changing weapon that uses radio waves to disable enemy electronics and take down multiple drones at once is under development for the U.K.'s armed forces.

This forms part of the work to put the U.K.'s defense industry on a war footing following the Prime Minister's announcement of an increase to the defense budget to 2.5 percent of GDP by 2030.

An example of a Radio Frequency Directed Energy Weapon (RFDEW), the versatile system can detect, track and engage a range of threats across land, air and sea. The system will be able to effect targets up to 1 km away, with further development in extending the range ongoing. It beams radio waves to disrupt or damage the critical electronic components of enemy vehicles causing them to stop in their tracks or fall out of the sky.

At only 10p per shot fired, the RFDEW beam is a significant cost-effective alternative to traditional missile-based, air defense systems, capable of downing dangerous drone swarms with instant effect. The high level of automation also means a single person can operate the system. This technology can offer a solution to protection and defense of critical assets and bases.

RFDEW (Source: Ministry of Defence (U.K))

RFDEW technology can be mounted on a variety of military vehicles and uses a mobile power source to produce pulses of RF energy in a beam that can rapidly fire sequenced shots at individual targets or be broadened to simultaneously engage all threats within that beam.

The advanced technology is being developed by a joint team from the Defence Science and Technology Laboratory and Defence Equipment & Support, working with U.K. industry under Project Hersa. The next steps for RFDEW is undergoing extensive field testing with British soldiers over the summer.

DARPA Shows Concepts for the Future of VTOL Uncrewed Aerial Systems

Defense Advanced Research Projects Agency's (DARPA) AdvaNced airCraft Infrastructure-Less Launch And RecoverY program (ANCILLARY) shows six design concepts for a low-weight, large-payload, long-endurance vertical take off and landing (VTOL) uncrewed X-plane. The innovative configurations and critical technology designs come from a wide array of performers, from small start-up to legacy aerospace companies, broadening the network of partners contributing to the program.

"The goal of ANCILLARY is to increase small VTOL uncrewed aerial system (UAS) capabilities by a factor of three over the current state-of-the-art flying today," said Steve Komadina, DARPA program manager for ANCILLARY. "Our performers are searching for innovative ways to increase payload weight and range/endurance of small, ship-launched UAS by means of novel configurations, propulsion and controls while also removing the need for special infrastructure."

In Phase Ib, performers will continue risk reduction design, analyses, and tests for an X-plane demonstrator to prove out technologies for a future operational UAS that can be deployed and retrieved from Navy ships without the large mechanical launchers and landing/recovery equipment used today. The small UAS will need to takeoff and land vertically, like a helicopter, from ship flight decks and out-of-the-way land locations in most weather conditions but fly missions like a very efficient winged aircraft while carrying significant payload when needed.

"A network of these small UAS can be launched from a ship to provide beyond-line-of-sight F2T2 (find, fix, track, target) of surface vessels of interest for the ship commander," Komadina said. "While we anticipate this effort is most likely to support Navy and Marine missions, we have found other services are very interested in the capabilities this technology can bring to diverse missions, including logistics, strike and special uses by the Army, Air Force, Special Operations Command and Coast Guard."

X-plane (Source: DARPA)

"We expect the operational capabilities provided by ANCILLARY will be augmented by other technologies being developed within the Department of Defense's various research and engineering organizations, such as advances in sensors, electronic warfare and especially autonomy and artificial intelligence," said Komadina.

In Phase Ia, the ANCILLARY team explored conceptual designs from nine non-traditional and traditional military companies.

In Phase Ib, six companies — AeroVironment, Griffon Aerospace, Karem Aircraft, Method Aeronautics, Northrop Grumman and Sikorsky — will mature X-plane designs, with concentration on reducing system

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risks through refined higher fidelity design and analysis and by conducting component and configuration hover testing. At the end of this 10-month phase, teams will submit competitive proposals for Phase II detailed design, fabrication and flight testing.

The project is expected to culminate with X-plane flight tests starting in early 2026.

DARPA THREADS Program to Boost Effectiveness of RF-Based Applications

The Defense Advanced Research Projects Agency (DARPA) has awarded BAE Systems' FAST Labs™ research and development organization a $12 million contract for the Technologies for Heat Removal in Electronics at the Device Scale (THREADS) program.

The DARPA THREADS program aims to overcome the temperature limits at the transistor scale inherent to power-amplifying functions. With new materials and approaches to diffusing the heat that degrades performance and mission life for MMICs, THREADS aims to resolve the thermal management challenges of today's GaN devices.

Many military systems leverage RF electronics and have historically operated at powers well below their theoretical limits because the GaN transistors get too hot. Solving this challenge will improve the range of RF-based systems by nearly three-fold. This will expand engagement distances for warfighters — taking them further out of harm's way.

"Excessive heat in electronics has been a long-standing challenge in the aerospace and defense industry," said Caprice Gray, director of device materials and manufacturing research at BAE Systems' FAST Labs. "With material and process enhancements, we are on the verge of overcoming this challenge and doing so will unleash the hidden potential in mission critical electronic warfare and other RF-based systems."

BAE Systems will leverage its expertise and track record of developing and manufacturing advanced microelectronics for the program at its Microelectronics Center (MEC) located in Nashua, N.H. The MEC is an accredited Department of Defence (DOD) Category 1A Trusted Supplier and manufactures GaN and GaAs ICs in production quantities for critical DOD programs.

Work on the THREADS program includes collaboration with Modern Microsystems, Penn State University, Stanford University, University of Notre Dame and University of Texas at Dallas.

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SSG-30GHP-RC	10 MHz to 30 GHz	-47 to +28 dBm
SSG-44G-RC	100 MHz to 44 GHz	-40 to +17 dBm

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Mini-Circuits

Electromagnetic Metamaterials Market to Approach US$15B by 2034

Metamaterials use regular engineered patterns of subwavelength structures to interact with waves. Electromagnetic (EM) metamaterials promise to have transformative effects within the fields of optics and telecommunications. They could make biometric recognition cheaper and more accurate, make virtual reality more immersive and comfortable and facilitate high speed mobile internet with zero signal blackspots, yet adoption is in its infancy.

In "Optical & Radio Frequency Metamaterials 2024-2034: Markets, Players, Technologies," IDTechEx comprehensively examines the emerging technology of EM metamaterials in its second edition of this report. Drawing from interviews with companies across the value chain and IDTechEx's existing research on optical, telecommunication and emerging materials, the report evaluates the optical and RF metamaterials market in various applications, analyzing each application's requirements, and case studies of existing players.

The report identifies reconfigurable intelligent surfaces (RIS) in telecommunications and metalenses in smartphone cameras as significant opportunities. Through detailed segmentation, it presents a comprehensive overview of the status and market potential of each application. The forecast predicts the overall market to reach US$14.9 billion by 2034, driven by improved biometric sensing in smartphones via metalenses and increasing 5G mmWave rollout growing adoption of RIS.

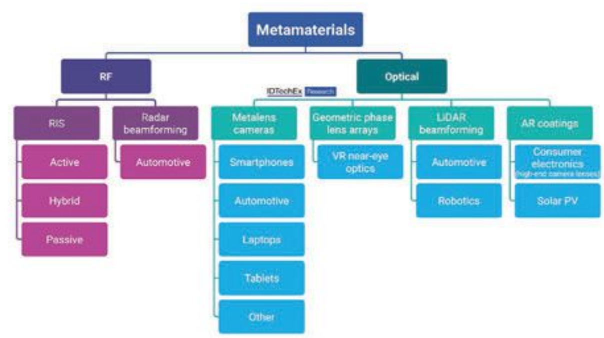
RF metamaterials find applications across multiple sectors, and can be utilized in RIS to reflect, steer and shield EM radiation, compensating for the reduced range associated with higher frequency signals. Additionally, in radar beamforming, RF metamaterials enable active steering of EM radiation to enhance angular resolution. This could be particularly beneficial for automotive radar systems. RF metamaterials can also be used for effective EMI shielding, enhancing security by preventing signal leakage, and can be frequency selective to create transparent shields. RF metamaterials also hold potential for medical sensing applications such as MRI scans and non-invasive glucose monitoring.

According to IDTechEx's forecast, the largest market for RF metamaterials is forecasted to be in RIS for 5G mmWave and future 6G communications. Both 5G mmWave and 6G offer significant advantages, including the potential for leveraging expansive bandwidth to support peak data flow ranging from gigabits to terabits per second and maintaining ultra-low latency.

However, utilizing high frequency spectra presents challenges such as very short signal propagation range (cm range for above 100 GHz frequencies) and line-of-sight obstacles. Addressing signal decay and establishing strong communication over reasonable distances is a priority for both technologies, especially in busy urban areas where consistent connectivity despite barriers is crucial.

Establishing numerous base stations is not cost-effective in providing adequate coverage for high frequency spectra like 5G mmWave and 6G. In contrast, metamaterial RIS can reflect and direct signals to end users, increasing signal range and strength while consuming low energy. Additionally, integrating metamaterial-based coatings with windows can improve signal coverage by reflecting beams around obstacles in urban areas. These solutions provide wide area coverage and offer vast opportunities for materials integration.

Relatively simple optical metamaterials based on biomimicry of moth-eye structures have a relatively long history of use as antireflective coatings in high-end camera lenses. However, metalenses fabricated using semiconductor industry processes are expected to have a huge impact, initially driven by their ability to improve the performance of computer vision systems.



Metamaterials (Source: IDTechEx)

Unjammable Sat-Navs and the Quantum Sensor Revolution

The modern world depends heavily on global positioning system (GPS) satellites to navigate, but too often, access to them is lost or even jammed. This creates a significant risk to safety in multiple industries, especially aerospace, but also automotive and consumer electronics.

Following the world's first successful flight demonstration of quantum navigation technology in May 2024 by BAE, QinetiQ and Infleqtion, this article outlines the power of quantum sensors. The quest for more reliable precision navigation and timing technology solutions is now driving significant interest in quantum sensors and atomic clock technology.

Quantum sensors use quantum phenomena to enable highly sensitive measurements of many physical properties. They can measure time (atomic clocks), magnetic field and current, gravity, angular motion, single photons and more. Emerging quantum tech-

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nologies within the quantum sensors market are also benefiting from the growing hype around quantum computing and quantum communication technologies (particularly given their applications for cybersecurity).

To date, the most common method to accurately determine one's position and the local time is via data from a global navigation satellite system (GNSS), for example, the U.S. military's GPS. However, there are environments where access to GNSS data is restricted. This can be a result of highly mountainous terrain blocking signals or spoofing by a third party. Precision navigation systems are under increasing pressure to remain reliable in GNSS denied environments.

Continuing to navigate when triangulation capabilities are lost depends on accurate measurements of distance traveled, direction, speed and time. Existing motion sensors, gyroscopes and local oscillators (clocks) do not have sufficient accuracy for precision navigation. The promise of quantum sensors and atomic clocks is that they are fundamentally much more accurate than traditional approaches, so much so that they can provide local access to precise inertial navigation systems without depending on GNSS.

There is now a range of atomic clocks that use high frequency oscillations between atomic energy levels commercially available, as well as others under development aiming to offer even higher accuracy measurements of time, from players such as Microsemi, Teledyne, Infleqtion and more. Similarly, quantum gyroscopes can use the sensitivity of quantum properties, such as spin, to determine rotation with a high degree of accuracy. Others are even investigating the potential of quantum gravimeters and quantum magnetic fields sensors for mapping and navigation applications.

Starlink (Source: IDTechEx)

There are multiple hardware approaches to manufacturing quantum technology for a variety of sensing applications. The method championed by Infleqtion in a recent flight demonstration with BAE is 'ultra-cold atoms.' Lasers can be used to trap atoms which makes their energy levels so low it has a cooling effect. In this state, the quantum properties of the atoms can be manipulated to make precise measurements. With specialized magneto-optical traps, ultra-high vacuum cells, ion pumps, rubidium atom sources and optics, Infleqtion has been able to decouple measurement of position from the environment completely and contribute to omitting the dependence on GPS to navigate within a plane.

Around the **Circuit**

Barbara Walsh, Multimedia Staff Editor

MERGERS & ACQUISITIONS

Quantic® Electronics, a portfolio company of Arcline Investment Management, announced the acquisition of **M-Wave Design**, a leading supplier of ferrite-based RF and microwave components for aerospace, defense and quantum computing applications. Founded in 1988, M-Wave designs and manufactures passive waveguide and coaxial components, including isolators, circulators, adapters and terminations. The company has a long history of supporting leading-edge development in high power and low loss passive designs. M-Wave's product portfolio is uniquely positioned to supply components that perform at cryogenic temperatures used in quantum computing applications.

NEW STARTS

Valvo Bauelemente GmbH, of Hamburg, Germany, a leading European manufacturer of high-power microwave and RF components, announces it is rebranding and unveiling a new name, **Microwave Techniques GmbH**. This announcement comes as part of a strategic alignment with its parent company, Microwave Techniques LLC, a global leader in high-power microwave and RF solutions. In 2023, Microwave Techniques acquired Valvo (now Microwave Techniques GmbH), to take advantage of synergies across teams, facilities, products and resources in the U.S. and Germany. Since then, the combined company has continued exploration of advanced research and development of its design, engineering and manufacturing of circulators, isolators, loads and windows, as well as further innovations for various high-power microwave and RF components product lines.

Intelliconnect (Europe) Ltd. opened their new base for sales, marketing and engineering in Witham, Essex, with a celebration of their innovation, achievements and future aspirations. The new facility is poised to be a hub of innovation and excellence, providing a base for long-term company growth and will be home to engineering, sales, administration and marketing and feature an exhibition area and conference suite. It will also be available for other Trexon group companies to use as a European base.

ACHIEVEMENTS

At the recent Conformance Agreement Group (CAG) meeting #78 of the Global Certification Forum (GCF), **Rohde & Schwarz** verified non-terrestrial networks (NTNs) NB-IoT test cases for RF and radio resource management (RRM), successfully meeting all test platform approval criteria. The R&S TS-RRM and R&S TS8980 test platforms were approved for every type of NTN NB-IoT test (RF, Demod and RRM), making Rohde & Schwarz the only company to have activated both NTN NB-IoT RF and RRM work items in the GCF. NTNs are wireless communication systems that operate above the Earth's surface. They are essential to realizing ubiquitous connectivity, bringing coverage even to remote areas that do not have access to traditional terrestrial networks.

BAE Systems has been selected by the **U.S. Navy** to develop Dual Band Decoy (DBD), one of the most advanced RF countermeasures in the world. DBD is a cutting-edge RF self-protection jammer that shields fighter jets from enemy attacks. Expanding the capabilities of BAE Systems' combat-proven AN/ALE-55 fiber-optic towed decoy, DBD consists of a towed unit connected by fiber-optic cable to electronic warfare equipment onboard the aircraft. The decoy delivers the latest jamming technology to disrupt enemy radars and lure missiles away from the aircraft. DBD can be launched by the pilot or automatically in response to threats, offering critical protection in highly contested airspace.

CONTRACTS

The **U.S. Army** awarded **Lockheed Martin** a $756 million contract to deliver additional capability for the nation's ground-based hypersonic weapon system, the Long-Range Hypersonic Weapon (LRHW). Under the new contract, Lockheed Martin will provide additional LRHW battery equipment, systems and software engineering support and logistics solutions to the Army. LRHW will introduce a new class of ultra-fast and maneuverable long-range hypersonic missiles with the ability to launch from ground mobile platforms. The LRHW weapon system is designed to launch the common hypersonic All Up Round (AUR), provided by the U.S. Navy-managed Conventional Prompt Strike program, includes the Army canister, a battery operations center and transporter erector launchers.

Leonardo DRS Inc. announced that it was awarded a contract from **NAVSEA** to provide AN/SPQ-9B radar design agent and engineering services. The contract includes options, if exercised, would bring the cumulative value to more than $26 million. Under the contract, DRS will provide system engineering, software development, hardware design, installation, safety, test, product updates, system upgrade and configuration management support. The AN/SPQ-9B is an X-Band, pulse Doppler, frequency-agile radar that was designed specifically for the littoral environment. It has a very high clutter improvement factor, supporting a very low false track rate in the littorals and in high clutter environments.

Stellant Systems Inc. recently was awarded two CFA contracts totaling $7.5 million. Both awards support the Aegis program and are procured by the **Naval Surface Warfare Center (NSWC) – Crane Division** and **Naval Supply Systems Command (NAVSUP)**. The Aegis Combat System is the Navy's most modern surface combat system. It was designed as a complete system:

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the missile launching element, the computer programs, the radar and the displays are fully integrated to work together. This makes the Aegis system the first fully integrated combat system built to defend against advanced air and surface threats. Additionally awarded was a $3.7 million contract from a major OEM for Stellant's Defense TWTs.

Lockheed Martin Canada has awarded **L3Harris Technologies** the Integrated Communications System for the Canadian Surface Combatant (CSC) of the Royal Canadian Navy (RCN), aimed at bolstering their operational efficacy and security on maritime missions. The CSC program, spearheaded by Irving Shipbuilding Inc., Lockheed Martin Canada and a consortium of partners, is a beacon of maritime innovation and revitalization within Canada's shipbuilding sector. With Irving Shipbuilding leading the construction efforts under the National Shipbuilding Strategy (NSS), Lockheed Martin Canada is at the helm of the design team, collaborating with L3Harris to integrate systems in Canada.

PEOPLE

▲ *Nathaniel Edington*

Filtronic, a global leader of high performance mmWave technologies for aerospace, defense, space and telecoms infrastructure markets, announced the appointment of **Nathaniel (Nat) Edington** as chief executive officer (CEO). As a veteran high-tech and semiconductor industry leader, Edington's previous roles include CEO of Dukosi Ltd. and Cambridge CMOS Sensors, along with strategic positions at AMS AG and Wolfson Microelectronics. These experiences have demonstrated his ability to drive technological innovation and corporate growth. Edington's appointment comes during a transformative period for Filtronic, which is set to expand its technological influence and manufacturing capabilities.

REP APPOINTMENTS

PEI-Genesis, a global leader in the design and assembly of custom-engineered interconnect solutions, has been named an authorized distributor for **CONEC** globally. This strategic partnership marks a significant milestone for both companies, amplifying their collective capabilities to serve diverse markets in the industrial sector worldwide. CONEC, a prominent member of the Amphenol Group, specializes in providing connector solutions tailored to demanding environments across a diverse array of industries. CONEC products serve as integral components within critical infrastructure worldwide, spanning automation, telecommunications, energy technology, machine manufacturing, agriculture, medical technology, transportation and the aviation industry.

INVITED PAPER

Using MEMS Switches to Characterize High Performance Antenna Tuning Devices

Mike Seibel and Brian Denheyer
NI, Austin, Texas

Tamir Moran
Menlo Microsystems, Irvine, Calif.

It is a perpetual challenge to evaluate the performance of next-generation technology with the current generation of technology. The test industry meets this existential challenge repeatedly by starting with a thorough understanding of the fundamentals that inform test methodology. That understanding guides the selection of technology that will accomplish the task at hand. This is the challenge of characterizing the harmonics and S-parameters of a next-generation, high performance antenna tuning switch (ATS).

Antenna tuning switches are used in broadband antennas to boost the efficiency of the antenna. Since the switches can be placed after the filters in the signal chain, they must be very linear to prevent generating harmonics that are within the passband of the antenna. Given the characteristics of the ATS being tested, the test system must be capable of measuring extremely low harmonic levels, on the order of -140 dBc, with a high-power fundamental signal level of about 10 W. The test system used to characterize the ATS is shown in ***Figure 1***, with the ATS configured for the through measurement and in ***Figure 2*** with the ATS configured for the shunt measurement.

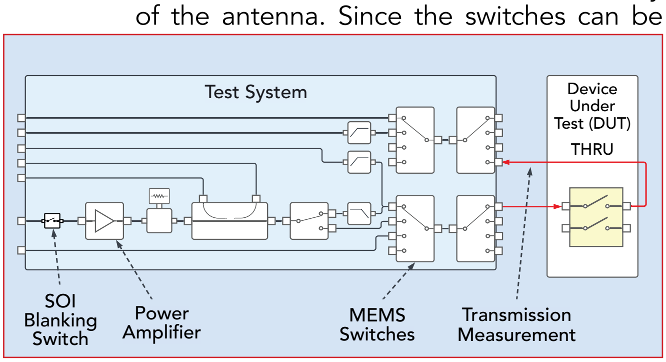


Fig. 1 **ATS thru measurement.**

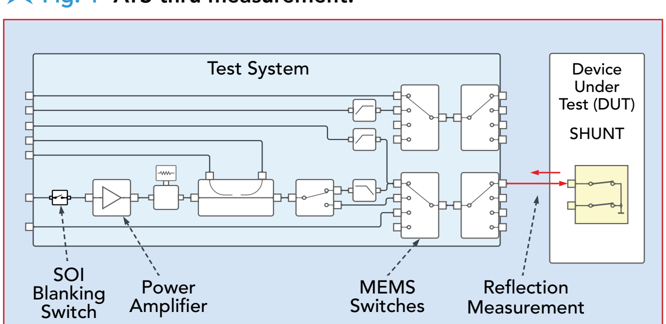


Fig. 2 **ATS shunt measurement.**

The test system used in both cases is an NI (now part of Emerson) Semiconductor Test System. It generates a high-power signal over an octave bandwidth and 10 W of power. The test signal is routed through a switch matrix to the device under test (DUT) and harmonics generated by the DUT up to 20 GHz are measured. It is desirable to connect to multiple DUTs at once to reduce the test time and test cost per DUT. The switch matrix creates a path from the power amplifier (PA) and receiver to each of the DUTs, separately, during the test sequence. The fundamental tone for harmonic measurements is generated by an NI PXIe-5842 vector signal transceiver and the setup has an NI PXIe-5632 vector network analyzer. This configuration can also perform S-parameter measurements of the DUT in either the shunt or through position.

The conditioning of the test signal begins with the PA, followed immediately by a circulator that provides a path to measure the power reflected due to amplifier mismatch. A forward coupler monitors and can be used to calibrate the output power. Lowpass filters are required to filter amplifier harmonics. A diplexer splits the band between the fundamental and the harmonics. A highpass filter provides additional filtering of the fundamental on the RX side of the diplexer. Because of the signal power, the amplifier and filter components are large and connectorized, requiring cable interconnects and all these factors combine to occupy precious space.

A drawback of having a flexible, multi-DUT connection capability is that it requires multiple switches. This architecture results in a switch tree in the signal path. Since these switches will attenuate the high-power signal, low insertion loss is important and using SP4T switches helps reduce the loss.

Multiple switches create linearity challenges. Each switch generates harmonics that will appear on the test signal and be reflected, affecting the measurement. Finally, a small form factor for the switches is essential to achieve the high connection density that the test system requires.

The methodology for testing high frequency ATS devices puts a burden on the switch. It must handle high power with low distortion, low loss, fast switching speed and have a small footprint. Having a switch that can provide a DC connection is essential as it allows both resistance and leakage measurements of the DUT. The best possible test results are heavily dependent on the switch selection. Selecting the correct component requires a thorough understanding of the available options.

SELECTING THE OPTIMAL SWITCH

A perfect switch has no resistance when biased on and infinite resistance when biased off. It switches instantly, requires no power to change states or to remain on, passes electrical signals from DC to light at any power level, is very small, lasts forever and costs nothing. However, this device does not exist, so switch advantages must be balanced against disadvantages to get as close as possible to the ideal switch. There are two main types of switching technologies used for high frequency applications: solid-state and electromechanical. There are options for each type:

Solid-state:
- Silicon-on-insulator (SOI)
- PIN diode
- GaAs field-effect transistor (FET)
- GaN FET

Electromechanical:
- Relays
- Micro-electromechanical systems (MEMS)

For solid-state switches, PIN diodes are current-controlled and FETs are voltage-controlled. Both can be implemented in different semiconductor processes like GaAs, AlGaAs, GaN and silicon. For FET-based switches, SOI and silicon-on-sapphire are also commonly used.

Using PIN diodes comes with a complex set of tradeoffs. Some of the key advantages are moderate RF power handling of several watts, switching speeds in the nanosecond to microsecond range, high isolation and IP3 values that can be greater than 45 dBm. Those advantages must be weighed against the disadvantages of DC power consumption that may exceed 100 mW per switch, low frequency operation that may not go below 50 MHz, larger overall circuit area and increased insertion loss created by additional passive bias components.

GaAs FET-based switches easily cover the desired frequency range and are widely used. GaAs FETs have switching speeds in the nanosecond range for 10 to 90 percent settling. That is sufficient for many systems, but gate lag can amount to several milliseconds. This decreases the usefulness of GaAs devices in precision test and measurement applications requiring signal stability and complete settling. GaAs switches suffer from lower RF power handling, typically in the 0.5 W range with higher insertion loss, especially for high throw count switches. The linearity is mediocre with IP3 values around 35 dBm and low P1dB performance.

GaN switch performance is similar to GaAs, but these devices can typically handle much higher RF power levels. GaN switches need control voltages in the 40 to 60 V range. Most GaN switches are also limited, in general, to a maximum operating frequency of 18 GHz. They also have similar switching characteristics to GaAs switches, including gate lag and they are generally more expensive.

Newer SOI devices are now gaining favor over commonly used GaAs switches because they exhibit much higher linearity and can provide Class 1C or greater ESD protection. However, higher operating frequencies require smaller devices, which affects the power handling of the switch. While the linearity of SOI switches is much higher than other solid-state switch technologies, it is still insufficient for many applications, including testing an advanced ATS.

Electromechanical (EM) relays work from DC to 50 GHz and beyond with minimal insertion loss, good return loss and high isolation. They can handle hundreds of watts and have extremely high linearity. However, EM switches consume hundreds of milliwatts of DC power when actuating, have switching speeds in the tens of milliseconds and are physically large, heavy and expensive. They also have comparatively short lifespans.

CHOOSING MEMS

After thoroughly evaluating various switches, MEMS switches stand out as the best choice. MEMS switches combine the performance advantages of EM switches with the miniature size, low cost, long life and scalability of solid-state switches. Ohmic MEMS switches operate by applying a DC voltage to the gate electrode. With no gate voltage, the beam is in its resting position as shown in ***Figure 3a***. When the voltage applied to the gate reaches the pull-in voltage, the beam or canti-

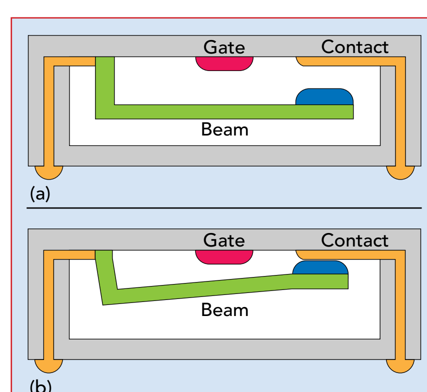


Fig. 3 (a) Ohmic MEMS switch in the open position. (b) Ohmic MEMS switch in the closed position.

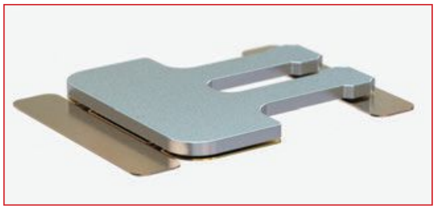


Fig. 4 **Menlo Micro's single unit cell ohmic cantilever design.**

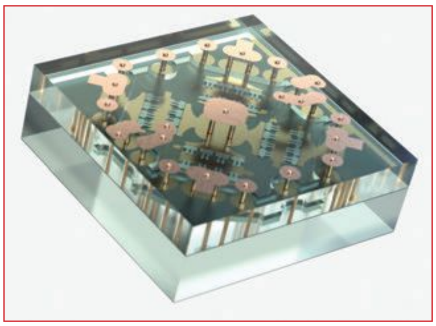


Fig. 5 **The Menlo Micro MM5130 SP4T switch.**

lever bends toward the contact due to electrostatic force and connects the input to the output, as shown in ***Figure 3b***. When the DC voltage falls below a pull-off level, the beam returns to its original position under its spring force. It is important to mention that while the pull-in voltage is in the tens of volts (DC), no power is consumed by the switch during actuation.

The Ideal Switch® from Menlo Micro is an ohmic cantilever design. The terminals of this MEMS switch can be viewed as a gate-source-drain transistor. In its simplest configuration, the switch is a single-beam, three-terminal device, acting as an SPST relay. This resembles an EM relay, but a MEMS switch is microscopic. The minimal size is highly advantageous. This 50 × 50 µm unit cell element, shown in ***Figure 4***, can easily be scaled into countless switching configurations with multiple throws and poles.

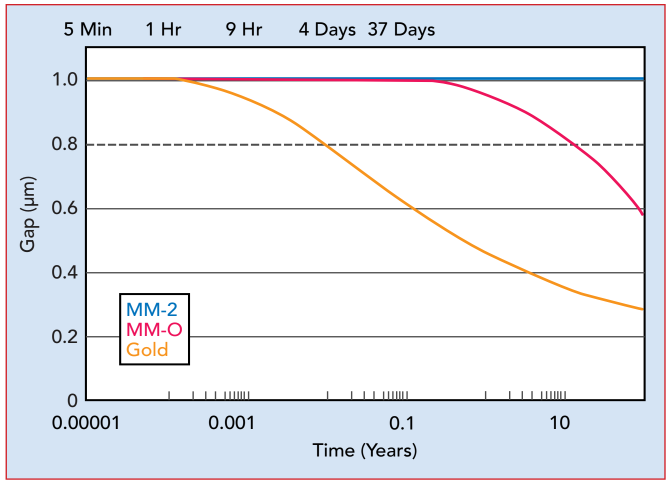
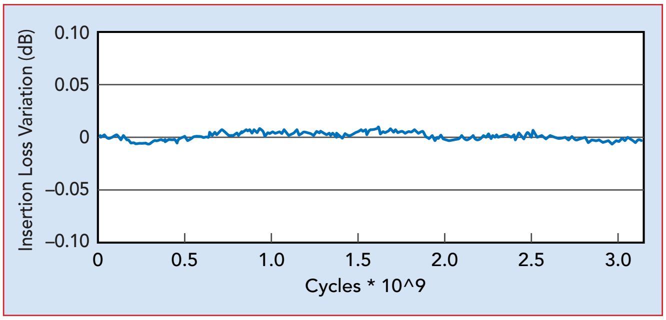


Fig. 6 **Switch deformation.**

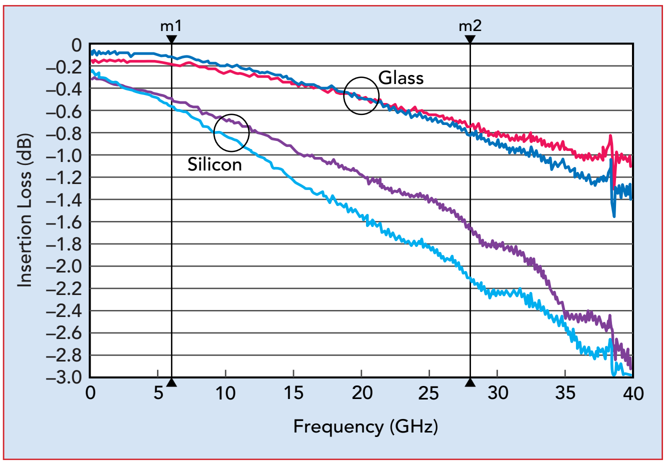
An SP4T MEMS switch from Menlo Micro was selected to meet the ATS test requirements. The device is shown in ***Figure 5*** in a glass wafer-level chip scale package. It was selected to take advantage of its small size, low loss, extremely high linearity and power handling performance. This switch has a single pole in the center of the die and four throws in the corners. Note that each arm of the switch is constructed from four parallel branches of unit cells to reduce the loss and increase its power handling.

A key to power handling and reliability is the proprietary electrodeposited alloys, which have mechanical properties similar to silicon with the conductivity of metal. These alloys exceed gold for strength and creep resistance. The specialized cantilever of the device design leads to longer life performance as indicated by the data shown in ***Figure 6***. This accelerated life test data shows how the initial 1 µm gap between the cantilever and the output contact collapses over time for a gold cantilever as compared to cantilevers manufactured with Menlo Micro's MM-0 and MM-2 alloys. In this case, the failure criterion is a gap below 0.8 µm. Note that the gap with MM-2 remains practically unchanged for well over 20 years.

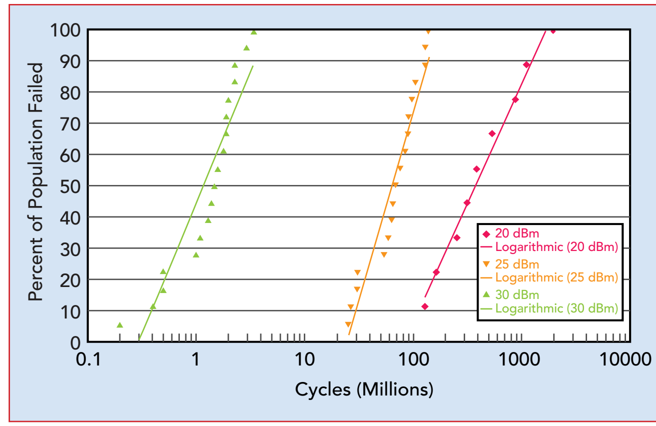
The materials used to provide stable and consistent contact performance over switch cycling and temperature are another critical aspect of this device. The switch uses a Ruthenium alloy along with a controlled atmosphere, which results in



▲ **Fig. 7** **Contact cycling with 10 dBm input at 25°C.**



▲ **Fig. 9** **Insertion loss comparison of different substrates.**



▲ **Fig. 8** **MM5130 hot switching.**

reliable operation for billions of cycles, as seen in ***Figure 7***, where insertion loss variations were monitored as the device was cycled. Note that the insertion loss was measured with an RF power of 10 dBm, indicating excellent reliability even with low levels of hot switching. Higher levels of hot switching are also possible if reduced life is acceptable as is evident from the measured data in ***Figure 8***. This plot shows the expected life of the switch when switching up to 30 dBm of RF power. Lifetimes of millions to hundreds of millions of cycles are achievable even with moderate levels of hot switching.

The Ideal Switch utilizes a through-glass via (TGV) process that enables a bumped, wafer-level chip scale package with a 2.5 mm × 2.5 mm form factor. The glass substrate is an important part of the performance improvement of the switch. ***Figure 9*** compares two SPST MEMS switches on glass with two switches on high-resistivity silicon substrates. The switches on the glass substrates show an improvement in loss of roughly 0.5 dB at 6 GHz and approximately 1 dB at 28 GHz. ***Figure 10*** shows an insertion loss comparison between the SP4T Ideal Switch, an SPDT SOI switch and an SPDT GaAs switch.

A glass substrate has additional benefits. It provides higher linearity than SOI switches that are built on high-resistivity silicon because it is a better electrical insulator and not a semiconductor. For reference, the IP3 of Menlo Micro's switches is typically greater than 95 dBm. The glass substrate also provides thermal stability that allows the electrical performance of the switch to remain unchanged over a temperature range of -55°C to +85°C. The harmonic performance of several different switch technologies is shown in ***Figure 11***.

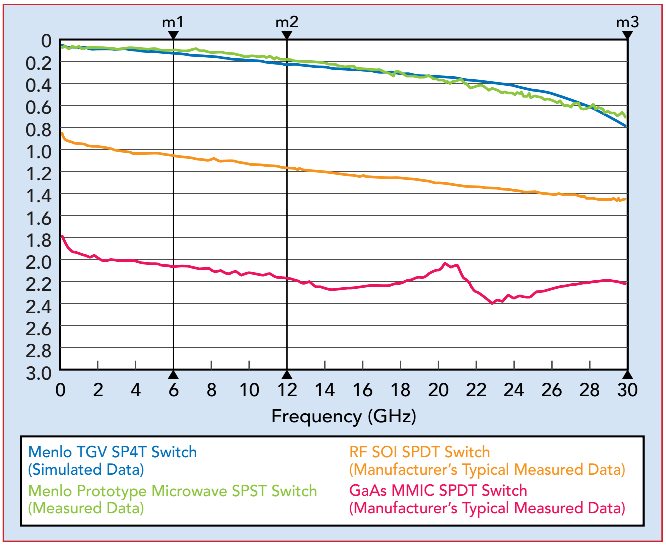


Fig. 10 **Insertion loss of different switch technologies.**

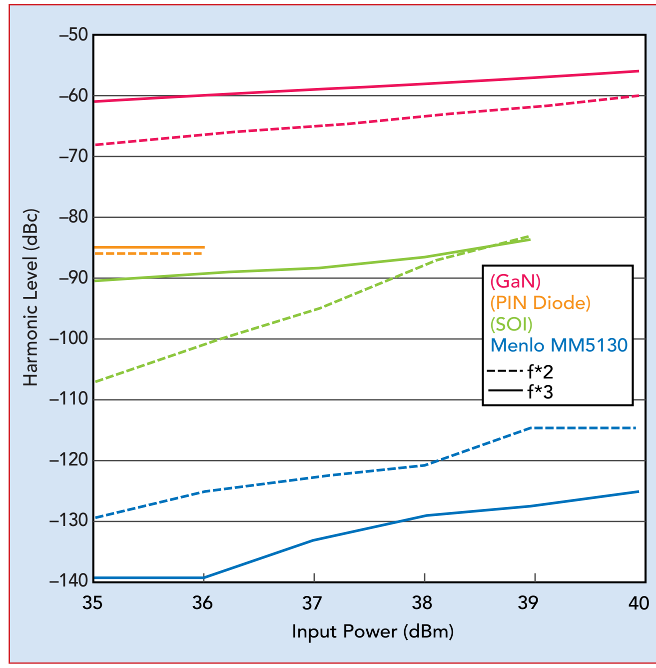


Fig. 11 **Second and third harmonic performance of different switch technologies.**

Table 1 shows the advantages and disadvantages of the different switch technologies for a variety of characteristics. While no technology is perfect, MEMS switches offer substantial benefits for a test system. The small size allows a large switch matrix to connect multiple DUTs. The low insertion loss reduces the RF power dissipation, maximizing the receive signal level. Although hot switching is a disadvantage of the MEMS switch technology, the Ideal Switch used in the test setup performs better than other MEMS switch offerings and the test system can control the test signal to avoid hot switching. The MEMS switch allows DC parametric measurements and the switching characteristics reduce test times.

USING MEMS IN ATS TESTING

Having settled on the switch, there are still testing challenges to address. The nominal HPA power is 10 W, corresponding to a peak voltage of almost 32 V into 50 Ω. The presence of an open or short, caused by the DUT or a problem in the path, can almost double the peak voltage. The component specifications must be checked against this worst-case peak voltage possibility. It is possible for components to handle the nominal power level but be underrated for the peak voltage experienced in a short or open condition. From here, the DC testing is relatively straightforward. The test voltage is less than one volt and the current is measured with a high-quality source measurement unit.

A minor drawback of MEMS switches is the presence of a shunt resistance when the switch is closed in addition to the shunt resistors required to prevent floating nodes. A simple calibration is required to accurately measure the resistance. The DC path also provides a simple and

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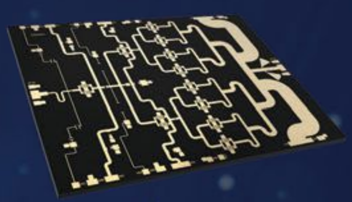
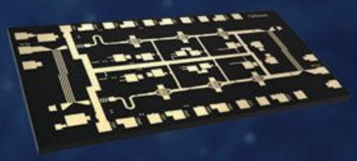
Ka

- NPA2001-DE | 26.5-29.5 GHz | 35 W
- NPA2002-DE | 27.0-30.0 GHz | 35 W
- NPA2003-DE | 27.5-31.0 GHz | 35 W
- NPA2004-DE | 25.0-28.5 GHz | 35 W
- NPA2020-DE | 24.0-25.0 GHz | 8 W
- NPA2030-DE | 27.5-31.0 GHz | 20 W
- NPA2040-DE | 27.5-31.0 GHz | 10 W



V

- NPA4000-DE | 47.0-52.0 GHz | 1.5 W
- NPA4010-DE | 47.0-52.0 GHz | 3.5 W



E

- NPA7000-DE | 65.0-76.0 GHz | 1 W
- NPA7010-DE | 71.0-76.0 GHz | 4 W*

* In Fabrication

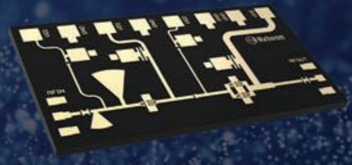


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TABLE 1

QUALITATIVE COMPARISON OF THE SWITCHING TECHNOLOGIES

	RF Power Handling	Size	Overhead	DC Power	DC Operations	ESD	Hot Switching	Linearity	Switch Life
SOI	Red	Green	Green	Green	Red	Green	Green	Yellow	Green
PIN	Green	Yellow	Red	Red	Red	Green	Green	Yellow	Green
GaAs FET	Red	Green	Green	Green	Red	Yellow	Green	Red	Green
GaN FET	Green	Green	Yellow	Yellow	Red	Yellow	Green	Yellow	Green
EM	Green	Red	Yellow	Red	Green	Green	Yellow	Green	Red
MEMS	Green	Green	Yellow	Green	Green	Yellow	Red	Green	Yellow

fast way to measure the continuity of the switches as a self-test to ensure the path is complete.

Since hot switching degrades the lifetime of a MEMS switch, test system techniques become important. Typically, a programmable device will ensure the RF input is disabled whenever a switch changes state. Developing a test system that allows control of the RF input is critical when using MEMS switches. In addition to the hot switching issue, many DUTs do not have appropriate heat sinks. To minimize these thermal issues, the duty cycle of the test may be adjusted to prevent overstressing the DUT.

Frequency harmonic levels for DUTs may be quite low, on the order of -120 dBc. In addition to the DUT, any active element in the test path will generate harmonics. As seen in Figure 11, this is a strength of the MEMS switches. The test system harmonic performance must be much better than the DUT being tested to prevent effects that will impact measurement accuracy.

CONCLUSION

The use of ATS in wireless systems is increasing. As the opportunities grow, the performance requirements get more difficult and this means test system performance must keep pace. Incorporating MEMS switches, along with a complex software framework into NI test systems is enabling the evolution of testing. Systems using these components and concepts have been successfully incorporated in production settings where these systems are providing the performance required to test leading-edge ATS products. Challenges remain, but architectures and configurations will evolve in response and MEMS switches will remain a vital part of this evolution. ■

INVITED PAPER

A Phase Noise Analysis Tool for Sparse Numerical Phase Noise Data

Shawn Logan
IEEE, Andover, Mass.

This article describes a phase noise analysis tool that creates a numerical model from discrete phase noise data. The tool includes an adaptive algorithm to identify spurious deterministic components in the data. It also creates a physics-based numerical model for the random noise component.

Despite its apparent simplicity, analyzing the temporal and Fourier characteristics of an oscillator from its phase noise characteristic presents challenges to designers and those wishing to specify an oscillator for an application.[1] Frequency spurs in the characteristic, measurement noise and a limited number of measured data points can significantly impact the accuracy of random and deterministic jitter components. To alleviate these difficulties, a phase noise analysis tool has been developed for use with measured or simulated phase noise data. Unlike other online and commercial phase noise analysis tools[2-5] that compute an integrated jitter value independent of the nature of the phase noise characteristic, this tool creates a numerical random noise model based on physical phase noise mechanisms to yield a more precise analysis. The tool algorithmically identifies and quantifies deterministic frequency components, which are removed to create the final model. The model makes the slope visible as a function of offset frequency to easily identify the physical nature of its noise components. The random and deterministic jitter components are computed using a bandpass filter with user-defined highpass and lowpass 3 dB corner frequencies. Computation of the jitter components using a brick-wall filter, a first-order filter or both is supported. Output data is provided in both graphical and tabular formats.

RANDOM PHASE NOISE NUMERICAL MODELING

Phase and Frequency Noise Sources

The sources of phase and frequency noise, although well recognized in measurement, are not fully understood.[6-8] The two most prevalent noise mechanisms are thermal noise and 1/*f* noise. The former represents Johnson noise, whose power spectral density, $S_f(f)$, does not vary with offset frequency. The latter is characterized by a power spec-

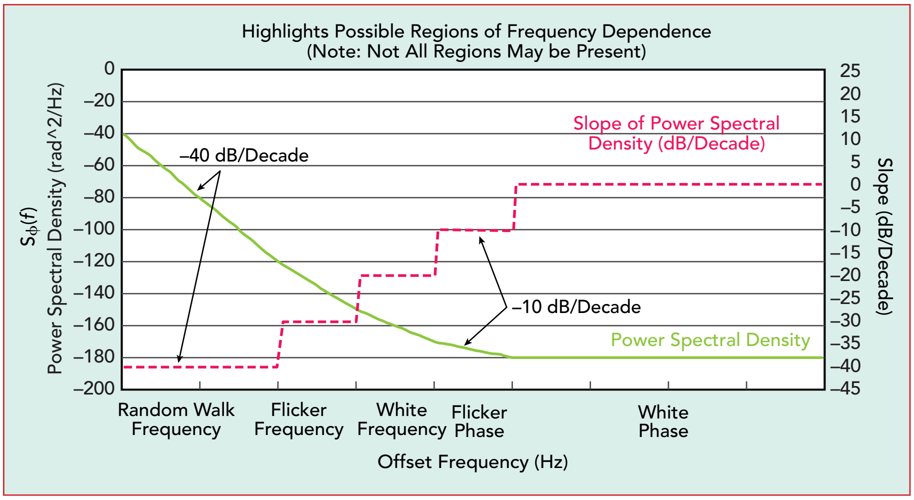

Fig. 1 **Power law dependencies of phase noise power spectral density.**

tral density that varies inversely with offset frequency from the carrier. It is often referred to as $(1/f)^b$ noise as it may present itself with an exponent b whose value differs from 1.

In the frequency domain, the general shape of $S_f(f)$, which includes thermal and $(1/f)^b$ noise sources and their slope, is shown in ***Figure 1***.[7,9] All 1/*f* noise mechanisms illustrated in Figure 1 may not be present in a given oscillator as the noise components of an oscillator may be dominated by one or two 1/*f* noise sources.

Random Phase Noise Modeling Considerations

There are offset frequency regions in Figure 1 where the relationship appears linear when the x-axis is logarithmic, but the entire curve cannot be well modeled by the linear relationship of ***Equation 1***:[10,11]

$$S_\phi(f) = c_0 + c_1 \log 10(f) \quad (1)$$

A second possibility is to consider an Nth-order polynomial model of the form shown in ***Equation 2***:

$$S_\phi(f) = \sum_{i=0}^{N} c_i [\log 10(f)]^i \quad (2)$$

A few disadvantages exist with this model choice. The first lies in the divergence of the model at the extrema of the phase noise data. The model is of limited use for extrapolating input phase noise beyond the offset frequencies of the data and this must be done with extreme caution. Second, as the order of the polynomial is increased to model phase noise more accurately over its entire offset frequency range, the function inevitably overshoots or undershoots when the slope of the phase noise characteristic changes. This can lead to a non-physical result and introduce significant errors in computations that use the model. Third, using an Nth-order polynomial model for phase noise in a curve-fitting algorithm, such as a non-weighted (or weighted) minimum squared error algorithm, presents difficulties since the phase noise at low offset frequencies far exceeds that at high offset frequencies. Even with a reasonable set of weighting factors, differences between the model and phase noise data at low offset frequencies dominate the differences at high offset frequencies. This results in a poor overall fit to the phase noise characteristic. Finally, the value of a high-order polynomial is extremely sensitive to numerical errors in its higher-order coefficients. Therefore, numerical precision is required for both its coefficients and its computation. Nevertheless, it is evident that over a limited offset frequency region of a phase noise characteristic, a polynomial-based model may provide a good estimate.

PROPOSED INITIAL RANDOM PHASE NOISE NUMERICAL MODEL

Given the limitations of a polynomial-based model and taking advantage of the inherent nature of phase noise sources, a multi-step curve-fitting algorithm has been developed. The initial model is compared to the phase noise data, and both are used to refine and produce a final random phase noise model. Instead of using an Nth-order polynomial model for the phase noise characteristic, the phase noise data is modeled with a cubic spline using a set of frequency-dependent logarithmic breakpoints determined by the minimum and maximum offset frequencies, f_{min} and f_{max}. The phase noise data is segmented into *S* adjacent segments where *S* is defined in ***Equation 3***:

$$s = ceil\left[\log 10\left(\frac{f_{max}}{f_{min}}\right)\right] \quad (3)$$

For example, if the phase noise frequency offset range spans 1 Hz to 500 kHz, the phase noise data is segmented into six regions; 1 to 10 Hz, 10 to 100 Hz...10 to 100 kHz and 100 to 500 kHz. Subject to the continuity constraints of a cubic spline, each of the phase noise segments is curve fit to a third-order polynomial, where the phase noise is expressed in dBc/Hz and the frequency axis is logarithmic. This forms the initial random phase noise model. This eliminates the disadvantages of using a high-order polynomial to model the entire phase noise characteristic. It also provides an innate smoothing of the phase noise characteristic if frequency spurs are present in the data. The tool takes full advantage of this smoothing operation.

DETERMINISTIC PHASE NOISE MODELING

The previous section outlined how to create an initial model of random phase noise in a timing reference from measured or simulated data. However, the presence of deterministic components in the phase noise characteristic impacts the accuracy of the random noise estimate. To create the most accurate model of random phase noise, deterministic phase noise components must be identified and removed from the data. To do this, an adaptive spur identification and removal algorithm has been developed that uses the initial cubic spline-based phase noise model and statistics derived from the phase noise data.

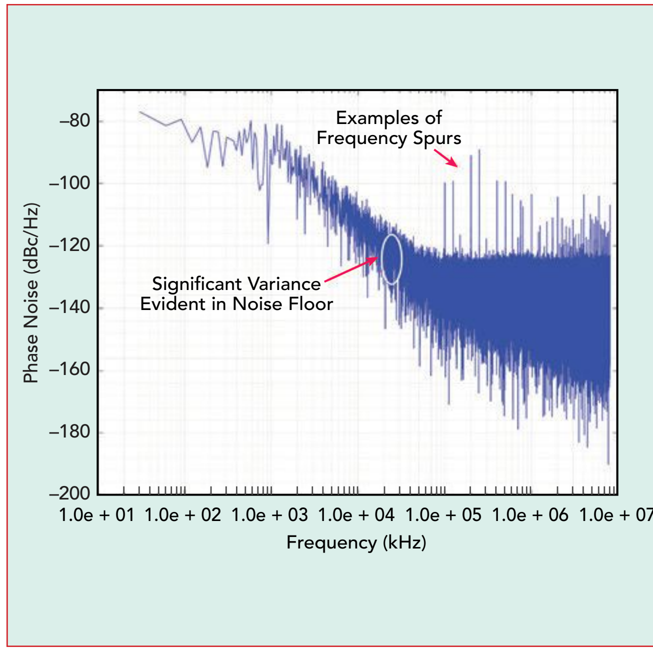

Fig. 2 **Phase noise of a 16 MHz phase-locked loop output with deterministic noise sources.**

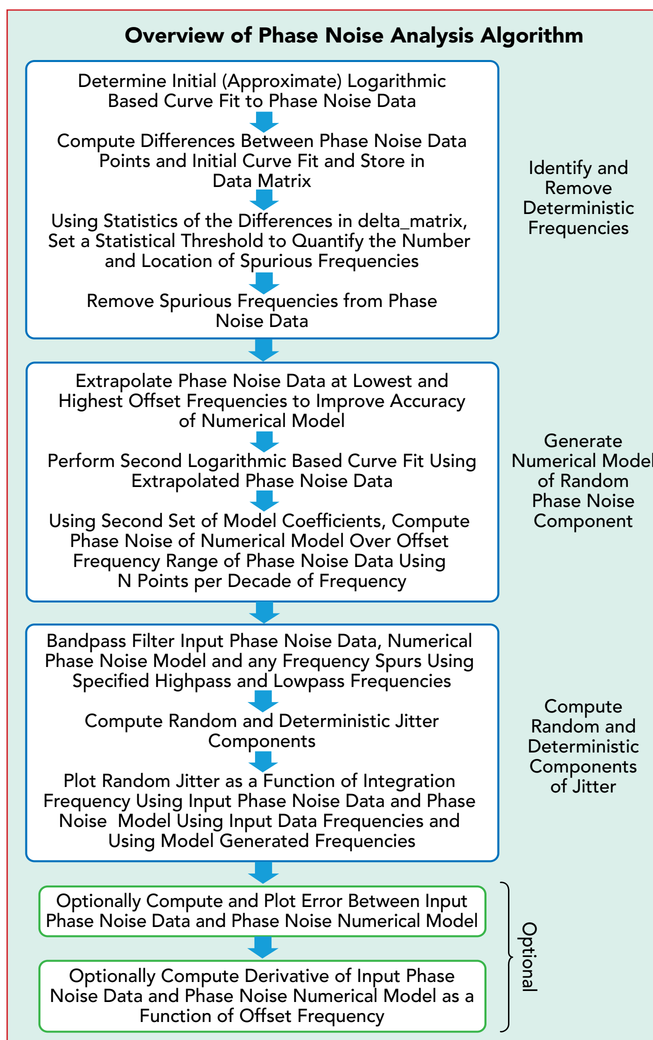

Fig. 3 **Phase noise analysis tool algorithm.**

Spur Identification and Removal Algorithm

Identifying a deterministic phase noise component, such as a frequency spur, depends on the magnitude and variation of the phase noise characteristic surrounding it. An example of a 12 MHz phase noise characteristic with both discrete spectral tones (spurs) and a deterministic noise source is provided in an Agilent E5052A signal source analyzer application note.[12] Selecting a single-phase noise threshold to identify a spur is not appropriate since the amplitude of a frequency spur can be far less than the amplitude of the random phase noise at low offset frequencies. In addition, identifying a frequency spur in a phase noise characteristic depends on the variance of the random phase noise floor surrounding the spur. While the variance of the phase noise floor in the application note[12] appears small, ***Figure 2*** illustrates the measured phase noise characteristic of a 16 GHz frequency reference where the variance of its phase noise floor is significantly higher. Therefore, accurately identifying the deterministic frequency components in a phase noise characteristic requires knowledge of the relative magnitude of the component and the noise floor surrounding the component.

To allow for both, the statistics of the phase noise data and the initial cubic spline-based fit of the random phase noise are used to identify and remove deterministic frequency spurs and components. The difference between the initial cubic spline-based curve fit and the actual phase noise data points is computed for each input data frequency. The rms value of the differences and the rms value of a subset of the differences that excludes the maximum difference values are computed. The set of difference values is divided by the rms value to convert it to peak-to-rms values.

The peak-to-rms value and the rms absolute value form the basis to set the threshold for identifying deterministic noise components. This results in an adaptive threshold for spur identification. The threshold for identifying a frequency spur for phase noise data with a large rms value noise floor is greater than for phase noise data with a small rms value noise floor. The frequencies and magnitudes of all spurious signals are tabulated with their rms values and replaced with values consistent with the random phase noise data and the initial curve fit to the random noise.

THE FINAL MODEL AND INTEGRATION

Completing the Random Phase Noise Model

The resulting "spur removed" phase noise data is combined with extrapolated phase noise data derived from the measured or simulated phase noise adjacent to its minimum and maximum offset frequencies. This improves the fit of the random noise model at the ex-

TABLE 1
INTEGRATED JITTER VALUE ERROR USING DIFFERENT ALGORITHMS

Phase Noise Data Points/Decade	Numerical Integration Algorithm		
	Trapezoidal (%)	Simpsons Rule (%)	Power Law (%)
1	236.39	230.19	-0.79
2	70.83	58.97	-1.05
4	20.20	8.68	-0.33
10	3.48	0.10	0.00

treme frequencies of the available phase noise data and enables limited extrapolation of the phase noise characteristic beyond the offset frequency range of the data. A second spline curve fit is performed on this extended dataset to produce the final random phase noise numerical model. The flowchart in ***Figure 3*** outlines the entire algorithm.

Computing Random Jitter from a Phase Noise Characteristic

The random jitter contribution of a timing reference is computed over some specified frequency bandwidth by integrating the bandpass-filtered phase noise characteristic. In the case of a brick-wall bandpass filter, the standard deviation (σ) of the random jitter in unit intervals (UI) is the integral of the phase noise $\mathcal{L}(f)$ between the lower and upper frequencies of the filter. This is shown in ***Equation 4***:

$$\sigma_{rms,UI} = \frac{1}{2\pi}\sqrt{\int_{f_{lower}}^{f_{upper}} 2\mathcal{L}(f)\,df} \quad (4)$$

For a bandpass filter with transfer function $H(f)$, offset frequencies are computed from the integral of the bandpass-filtered phase noise characteristic as shown in ***Equation 5***:

$$\sigma_{rms,UI} = \frac{1}{2\pi}\sqrt{\int_{0}^{\infty} 2H(f)\mathcal{L}(f)\,df} \quad (5)$$

Phase Noise Numerical Integration Algorithm

A power law-based interpolation to enable accurate interpolation of the phase noise between data points has been developed and implemented in a numerical integration algorithm. Since the physical mechanisms responsible for phase noise have a power law dependence, the relationship between the phase power spectral density, ($S_{\varnothing}(f)$), at frequency $f_o+\Delta f$ relative to its value at f_o may be described by ***Equation 6***.

$$\frac{s_{\phi}(f_o+\Delta f)}{s_{\phi}(f_o)} = \left(\frac{f_o}{f_o+\Delta f}\right)^{z}, z \geq 0 \quad (6)$$

In this expression, z is zero or a positive exponent associated with the phase noise mechanism(s). In general, z is not an integer.

The value of z for a set of two-phase noise points and their respec-

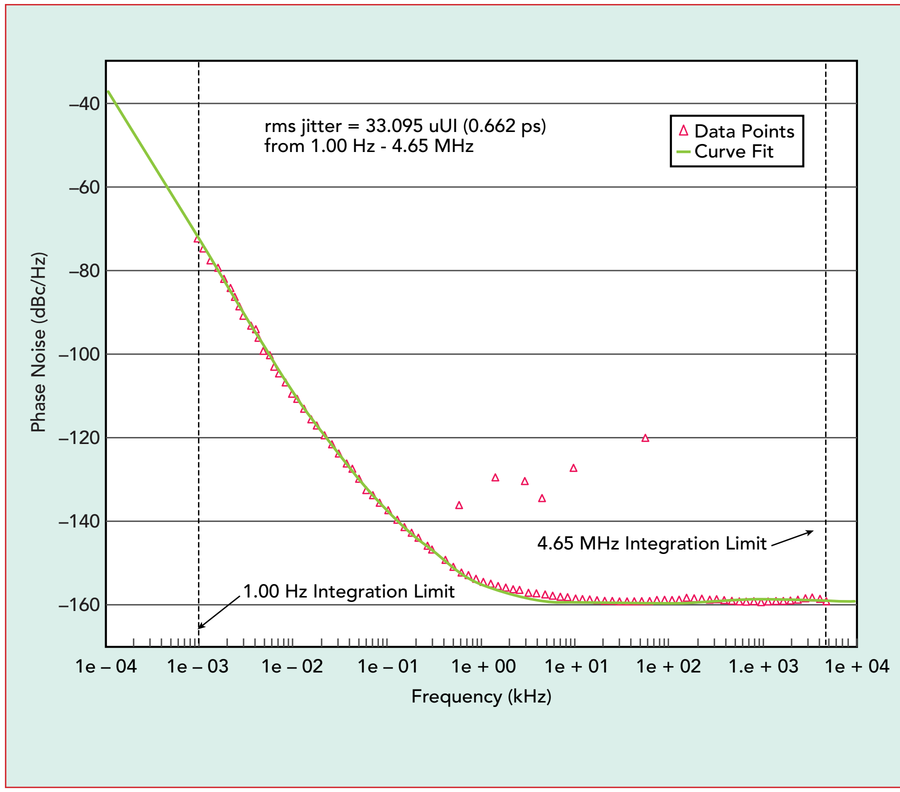

Fig. 4 50 MHz CMOS OCXO phase noise data[13] and random noise model.

tive offset frequencies is defined in ***Equation 7***:

$$z = \frac{\log 10\left[\frac{s_\phi(f_o + \Delta f)}{s_\phi(f_o)}\right]}{\log 10\left[\frac{f_o}{f_o + \Delta f}\right]} \qquad (7)$$

The expression for the integral of the spectral phase noise density between the two frequencies f_o and $f_o+\Delta f$ when $z \neq 1$ is defined in ***Equation 8***:

$$\int_{f_o}^{f_o+\Delta f} S_\phi(f)\left(\frac{f_o}{f}\right)^z df = \frac{S_\phi(f_o)}{1 - z} f_o\left[\left(1 + \frac{\Delta f}{f_o}\right)^{1-z} - 1\right] \qquad (8)$$

For $\left|\frac{\Delta f}{f_o}\right| < 1$, ***Equation 9***

$$\int_{f_o}^{f_o+\Delta f} S_\phi(f_o)\left(\frac{f_o}{f}\right)^z df = \frac{S_\phi(f_o)}{z + 1} f_o\left[1 + (1 - z)\left(\frac{\Delta f}{f_o}\right) + \frac{(1 - z)(-z)}{2!}\left(\frac{\Delta f}{f_o}\right)^2 + \cdots\right] \qquad (9)$$

expresses the integral as a converging binomial series. Inspection of Equation 9 indicates that the use of only the first-order or first- and second-order ($\Delta f/f_o$) terms to estimate the integral becomes less accurate as ($\Delta f/f_o$) increases. As a result, the accuracy of the integrated value of a phase noise characteristic using a trapezoidal algorithm (first-order) or Simpson's rule (second-order) algorithm will be poor for frequency steps large relative to f_o.

Table 1 shows the error between the 1 Hz to 10 MHz integrated jitter value of the phase noise characteristic of a 50 MHz oscillator using between 1 and 10 data points per decade of the phase noise characteristic with trapezoidal, Simpson's rule and the proposed power law algorithms. For fewer than four data points per frequency decade, the integrated jitter values using the trapezoidal and Simpson's rule algorithms have a significant error consistent with the limited accuracy of the linear- and quadratic-based interpolation algorithms predicted by Equation 9. This is evident in the integrated random jitter values provided by commercial phase noise analysis tools[2-5] that use linear or quadratic interpolation-based numerical integration algorithms.

SUMMARY

Phase Noise Modeling Tool Algorithm

The phase noise modeling tool uses a random noise modeling pro-

cess, a deterministic jitter identification and removal algorithm and a phase noise integration algorithm to analyze numerical phase noise data supplied in a comma-separated variable text file. This is shown in Figure 3. For the 50 MHz oven-controlled crystal oscillator (OCXO) phase noise characteristic[13] used as an example, ***Figure 4*** shows the phase noise data points and the curve fit. ***Figure 5*** shows the phase noise data with the spurs identified and ***Figure 6*** shows the slope of the phase noise characteristic computed from the data points and from the model.

The phase noise analysis tool creates a numerical model from discrete phase noise data. The tool includes an adaptive algorithm to identify spurious deterministic components in the phase noise data. It also creates a physics-based numerical model for the random noise component of the phase noise. The tool includes a means for integrating the phase noise model and input phase noise data using a brick-wall and first-order bandpass filter with

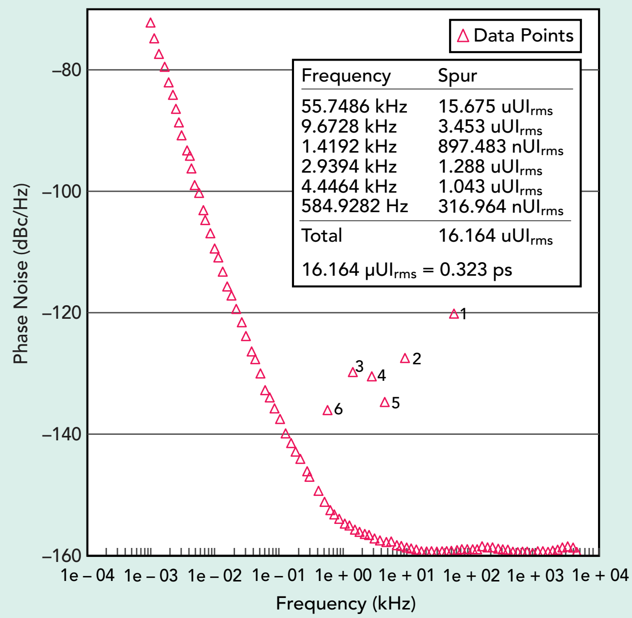

Fig. 5 **50 MHz CMOS OCXO phase noise data[13] with spurs identified.**

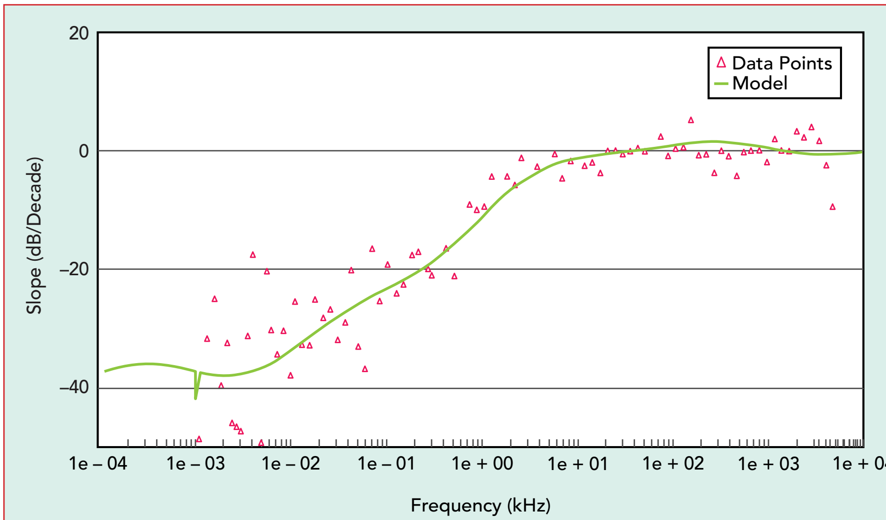

Fig. 6 **Slope of 50 MHz CMOS OCXO phase noise characteristic[13] and model.**

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a numerical integration algorithm developed to provide accurate integration of input phase noise data with as little as a single frequency/phase noise data point per decade of frequency.

Detailed program operation and case studies of measured and simulated sets of phase noise data to validate the accuracy of the model and its features are documented by the author.[14,15] The phase noise tool is implemented in Octave[16] and C and is freely available. ■

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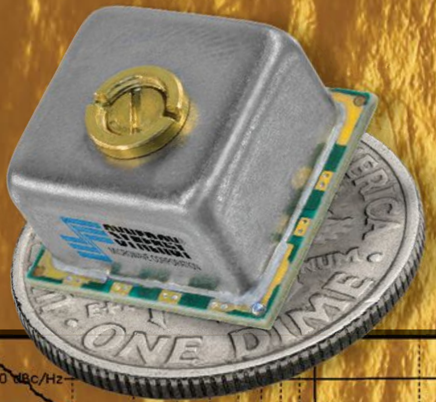

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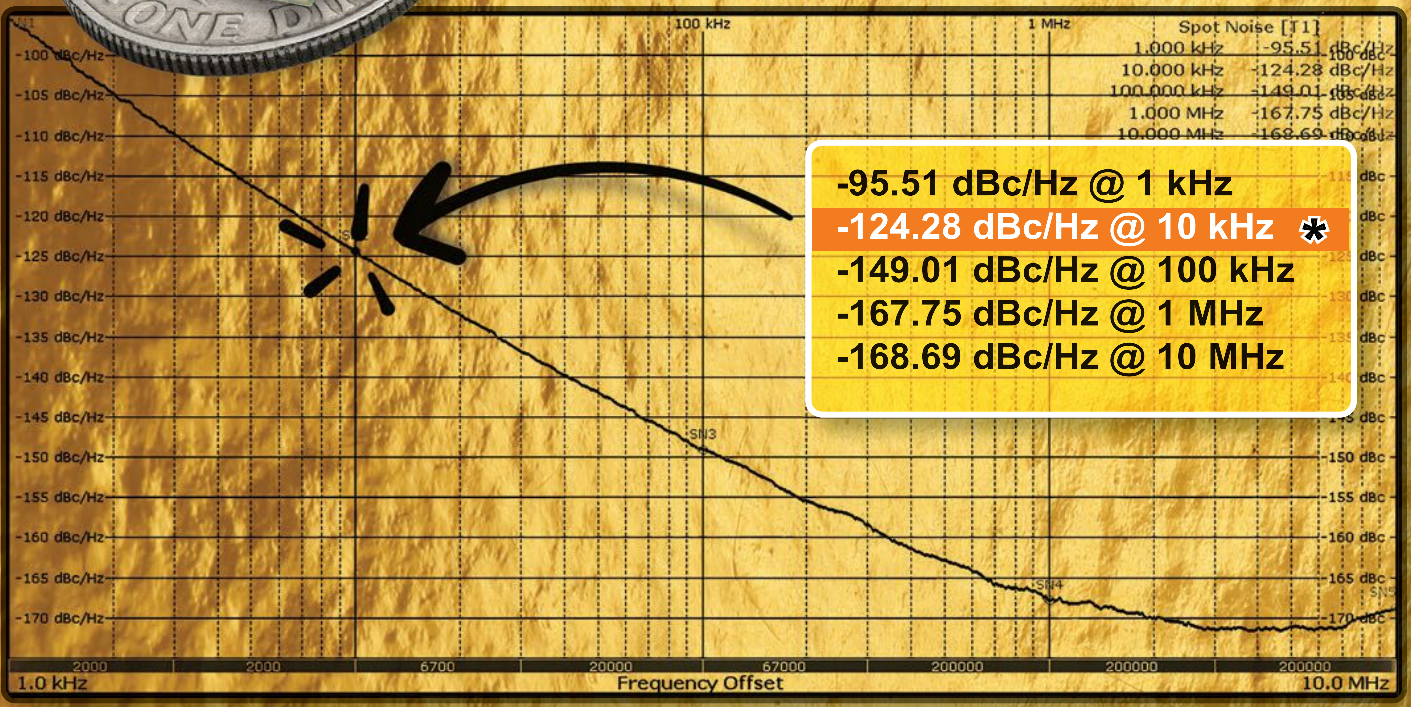

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INVITED PAPER

From Transistor Characterization to System-Level Application: A Complex but Tremendous Journey

Nicolas Labrousse and Wissam Saabe
AMCAD Engineering, Limoges, France

The evolution of telecommunications has been marked by a series of major transformations, with significant advances in key areas such as high-efficiency RF power amplifiers (PAs), wireless technology for 5G and beyond and the IoT. These advances have been made possible by improving transistor technology and the growing use of GaN HEMT transistors that achieve higher power density. These developments lead to more integration and support for the high frequency bands that are becoming mandatory for 5G and 6G applications. Using cutting-edge design tools and reliable simulation software allows engineers to develop initial designs accurately and efficiently. This article explores the impact of these advances in the telecommunications landscape. It will highlight different steps of the GaN HEMT transistor characterization and modeling processes, along with the application of these models for PA design. It will also address system application simulation using advanced measurement and simulation tools.

COMPACT MODELING FOR GAN HEMT TRANSISTORS

A "compact model" is based on electrical measurements. The advantages of this modeling approach are the high execution speed, the scalability and the possibility of adding additional influences. These influences may include things like external temperature and self-heating as well as trapping effects.

The typical topology of a GaN HEMT transistor is shown in ***Figure 1***.[1] The model is composed of extrinsic parameters that take into account gate and drain pad capacitances as well as gate, drain and source resistance and inductance characteristics. The model integrates linear and nonlinear models addressing capacitances, diodes and the output current source. An additional thermal model calculates the instantaneous dissipated power. This dissipated power is then used to evaluate junction temperature variation thanks to the multi-cell RC circuit. Finally, a trapping model is inserted to monitor the output current source according to transient phenomena like capture and emission.

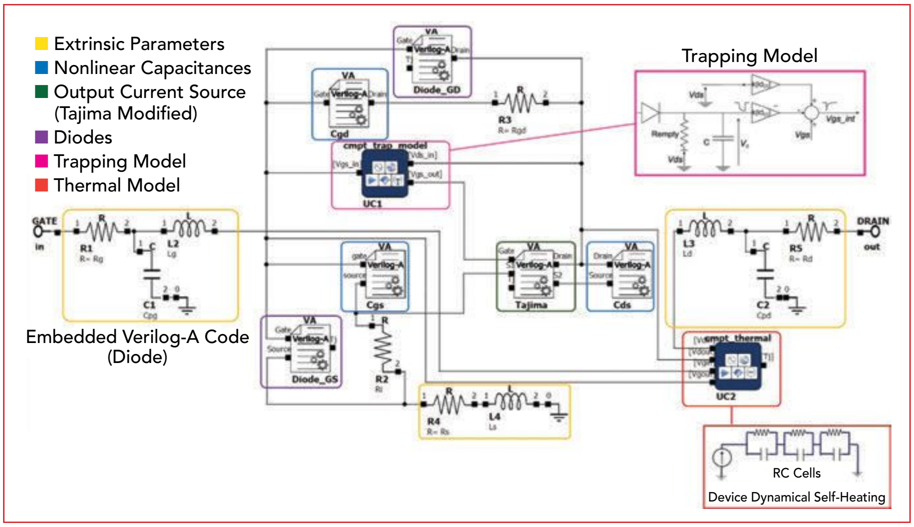
It is important to mention that the nonlinearities are modeled using Verilog-A code. This standard is widely used in many EDA tools, allowing easy transfer between different software platforms. With compact modeling extraction, it becomes necessary to perform various measurement types to extract the different model parameters.

CHARACTERIZING GAN HEMT TRANSISTORS FOR RF APPLICATIONS

The I-V characteristic is essential for estimating the performance of RF power transistors.[2] The characterization is carried out in a pulse-mode measurement to overcome self-heating. The pulsed I-V system is combined with a vector network analyzer (VNA) to obtain the scattering parameters for each pulsed bias point. Using this technique, it is possible to extract linear models from all the I-V characteristics and to derive the nonlinear model.

Thermal effects are key aspects of RF power transistors.[3] These effects are especially important when working with modulated signals that may have short- and long-term memory effects. Electrical methodologies have been developed to measure these thermal effects. These techniques are based on pulsed and/or DC I-V measurements done at different chuck temperatures. The aim is to characterize a given parameter, like on-resistance, gate or drain currents, as a function of the dissipated power and the chuck temperature.

The trap phenomenon is another important aspect to consider for GaN HEMT transistors. Traps have a significant impact on the achievable performance of GaN technology. These traps result from impurities or



▲ **Fig. 1** **GaN HEMT transistor model from a pre-release AMCAD compact modeling tool.**

defects in the crystal lattice or on its surface. A pulsed-mode measurement technique enables the characterization of the transient effects induced by traps in the component while avoiding thermal effects.

COMPACT MODEL EXTRACTION AND SIMULATION OF A GAN HEMT TRANSISTOR

The process of extracting a compact model is sequential and incremental. The process involves CAD software that may embed DC, AC, transient, harmonic balance and other different kinds of simulation engines. Using these tools, it is possible to compute the circuit response of the model in conditions close to those used in the actual characterization measurement.

The model extraction process starts with determining the linear and the nonlinear model elements.[4] These elements include the diodes, the output current source and the nonlinear capacitors. Then, thermal and trap models are added.[5] Thanks to transient simulations, the model response over pulsed stimuli can be obtained.

Finally, the model is compared against large-signal measurements obtained using a VNA-based load-pull system. Harmonic balance analysis is used to compute the periodic steady-state response to get the AM-AM and AM-PM characteristics for different load impedances and conditions close to the final application. ***Figure 2a*** shows a comparison between modeled and measured large-signal performance and contours at load impedances that result in 3 dB gain compression from the maximum output power. ***Figure 2b*** shows the same modeled and measured large-signal performance and contours at load impedances that result in maximum power-added efficiency at 3 dB compression. The measurements were performed at 3.6 GHz on a GaN-on-SiC HEMT device with four gate fingers and a 220 µm gate width. The contours show good agreement between the measured results and the model. The graphs showing output power (P_{out}), PAE, gain (G_p) and output current (I_{out}) are plotted as a function of delivered input power (P_{in}) for the specific load impedance.

These results are an invaluable source of information for the model engineer and the design engineer. From these results, the model may be adjusted to better match the actual results. Thanks to the versatility of the Verilog-A format, the model can be transferred to the design engineer at this step to complete the RF PA design.

TRANSISTOR-LEVEL TO SYSTEM-LEVEL SIMULATION

Recent advancements in EDA software have revolutionized the design of increasingly complex circuits. This has both enabled and accommodated the demands of increasingly sophisticated modern telecommunications technology. As an example, the adoption of advanced topologies like Doherty amplifiers boosts efficiency but further complicates design challenges. These tools now enable designers to meticulously simulate and optimize the performance of each component well before actual production begins. The aim is to harness all this preparatory work to enable comprehensive system-level evaluations that ensure that all components function harmoniously within the intended system architecture.

Behavioral models are essential throughout the design cycle of RF systems. Initially, these models facilitate the specification of system elements by creating a digital twin that guides the selection of suitable off-the-shelf components. As the design cycle progresses, these models become invaluable tools for developers of signal processing algorithms, digital predistortion techniques and control systems. These tools allow developers to test their solutions against realistic and comprehensive circuit impairment scenarios. This testing helps to ensure the effectiveness and robustness of the system. Finally, before system assembly, the digital twin is updated with the newly designed circuits, enabling a preliminary validation phase that incorporates measurements from various prototypes.

As an example of the utility of this approach, high peak-to-average power ratios (PAPR) in modern communication signals induce strong amplitude fluctuations. These amplitude fluctuations can lead to signal distortions when amplified by nonlinear devices like PAs. Behavioral modeling presents a scalable solution by allowing the characterization of the nonlinearity, memory effects and dynamic responses of a PA to varying signal conditions without the extensive overhead of physical prototyping.

PA BEHAVIORAL MODEL EXTRACTION AND SIMULATION

Starting from circuit designs in EDA tools, PAs can be modeled at the transistor level to ensure that every nuance of electronic interaction is captured. These designs are typically simulated under various conditions that may include sweeping the power and carrier frequency of the CW input signal and PA load impedance to generate comprehensive data sets that better describe the behavior of the amplifier. ***Figure 3a*** shows the measured versus modeled responses of the load-pull gain characteristics of a 2.65 GHz PA with parameterized load impedance. ***Figure 3b*** shows measured versus modeled agreement for the gain contours of that same amplifier at P_{in} = 23 dBm. The excellent agreement shown in both figures is, in part, due to the behavioral model that faithfully reproduces the nonlinear characteristics of this PA designed for telecom base stations. In addition to the nonlinear characteristics, the model also takes into account the mismatch that can be introduced in active antenna architectures.

These data form the foundation for behavioral model extraction, which abstracts the response of the PA into an object that can be used for system-level simulations. The extraction of behavioral models necessitates a thorough analysis of the PA, particularly to describe its response to modulated signals. These signals often exhibit variable envelopes that are affected by low frequency memory effects. Techniques like two-tone tests are instrumental in identifying the nonlinearity and memory effects that manifest over a range of frequencies and power levels.

In scientific literature, behavioral models like the Volterra series and

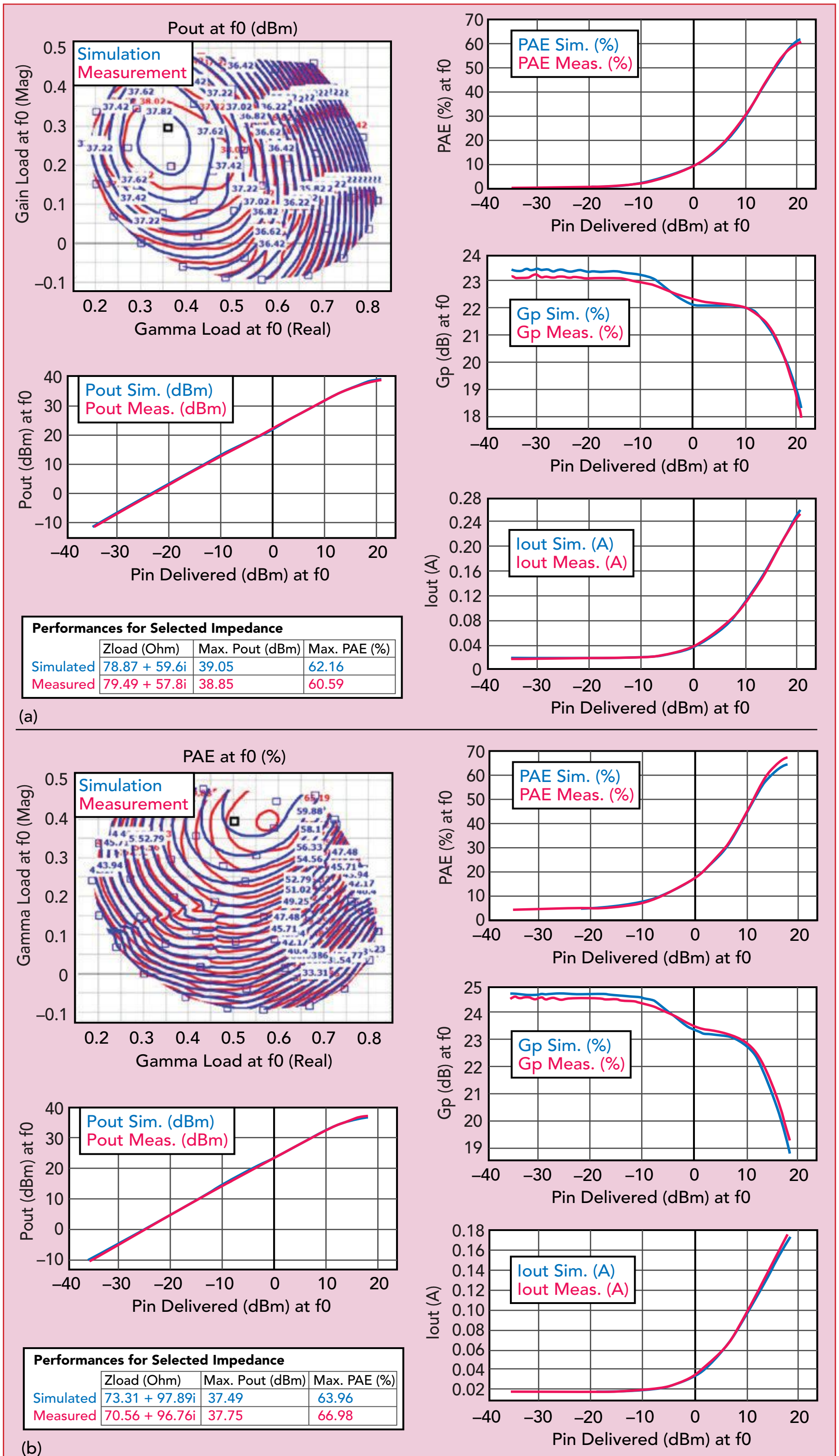


Fig. 2 (a) Large-signal performance at 3 dB gain compression. (b) Power-added efficiency performance at 3 dB gain compression.

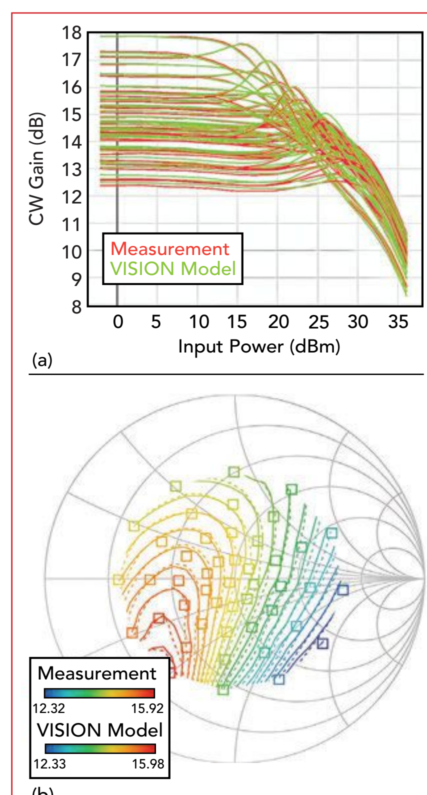


Fig. 3 (a) CW gain at 2.65 GHz. (b) CW gain contours at P_{in} = 23 dBm.

its truncated variants such as the Generalized Memory Polynomial (GMP) effectively capture the dynamics of a given signal and provide a suitable framework for use in PA linearization applications.[6,7] This requires extracting the model, whenever necessary, following variations in signal characteristics. For system simulation, another approach that is like the method used in transistor modeling is applied. This method consists of extracting the coefficients in one pass, characterizing the high frequency and low frequency memory effects separately. This is formally known as the Two-Path Memory (TPM) model or High-Power Amplifier Unilateral with High Frequency and Low Frequency Memory Effects (HPA-U-HFLF) model.[8] This method improves the robustness of the prediction by considering the various signal characteristics to which it will be exposed. This includes varying PAPR levels, from small-signal linear regimes to significant gain compression and a wide range of signal bandwidths from kHz to several GHz.

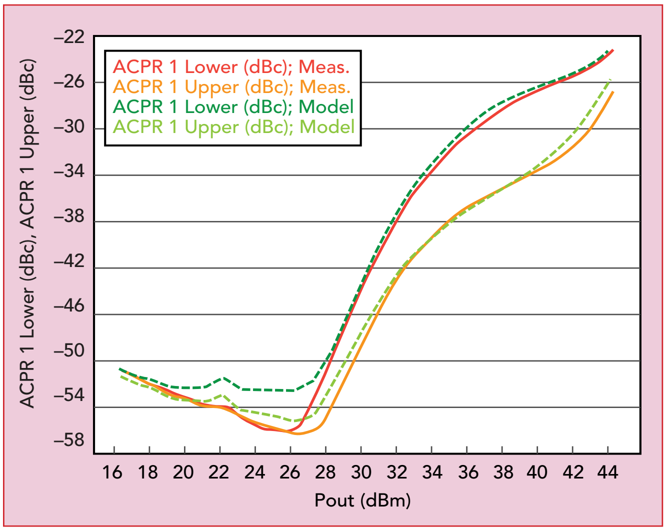


Fig. 4 Measured and modeled ACPR simulation.

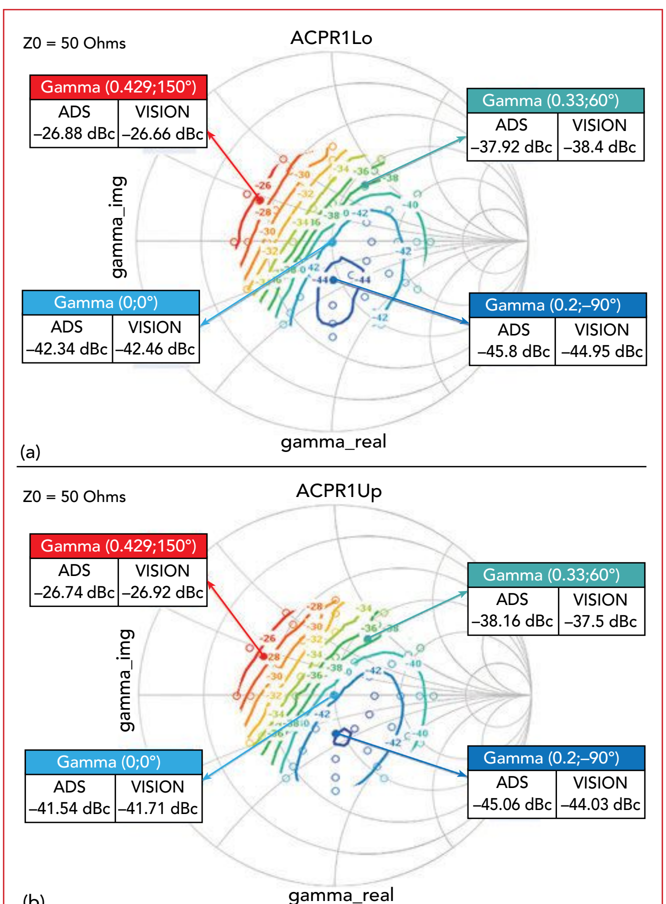


Fig. 5 (a) Lower ACPR simulation results. (b) Upper ACPR simulation results.

Figure 4 shows the measured and modeled ACPR results for the lower and upper channels of a PA stimulated by a 16-QAM signal, characterized by 4 dB PAPR and a bandwidth of 50 MHz. The results show an asymmetry highlighting the low frequency memory effects in the PA. They also show the ability of the behavioral model to predict these figures of merit over a wide average power range.

Recent work has made it possible to take into account nonlinearities, along with high and low frequency memory effects and mismatching in a single model. This enhanced TPM model, or the High-Power Amplifier Bilateral with High Frequency and Low Frequency Memory Effects (HPA-B-HFLF) model,[9] was first tested on a PA circuit designed in PathWave ADS software provided by Keysight Technologies. The model was extracted using harmonic balance simulations (load-pull and two-tone analysis) and validated in an envelope transient simulation using a 1024-QAM signal with a 160 MHz bandwidth. The signal, with a PAPR of 6.6 dB, is substantial enough to markedly stimulate the nonlinear response characteristics of the PA. ***Figure 5a*** shows the lower ACPR contours and ***Figure 5b*** shows the upper ACPR contours. ***Figure 6*** shows the EVM contours. These three plots use simulation results from the HPA-B-HFLF model, measured with an average input power of 10 dBm. This new behavioral model was tested with different load impedances and demonstrated an exceptional ability to predict spectral responses and key metrics, such as the ACPR results shown in Figure 5 and the EVM results shown in Figure 6 over a wide range of load impedances.

In addition to the performance evidenced by the

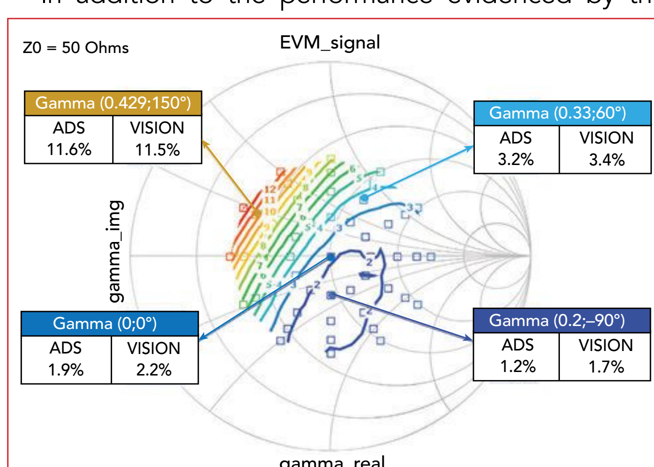


Fig. 6 EVM contours.

HPA-B-HFLF model, simulation times were deemed to be reasonable. This was particularly true when compared to the circuit-level simulation. For example, obtaining the ACPR and EVM contours took less than 10 minutes to simulate using the HPA-B-HFLF model. This is compared with one hour for a nominal simulation using the circuit design alone. This aspect of simulation time is one of the main reasons for using behavioral models.

CONCLUSION

The journey from GaN HEMT transistor characterization to the implementation of these devices in real-world systems underscores a significant advancement in telecommunications technology. This progression illustrates the crucial role of advanced modeling and simulation techniques in bridging the gap between microscopic electronic behavior and macroscopic system performance. By leveraging sophisticated compact modeling, engineers can predict and optimize the performance of PAs more accurately, leading to more efficient and robust telecommunication systems. Furthermore, the integration of behavioral models into the system-level evaluations not only enhances design accuracy but also reduces development time and costs, enabling faster market deployment. This comprehensive approach, from transistor-level analysis to the system-level application, is crucial for meeting the burgeoning demands of next-generation wireless technologies, ensuring that new telecommunications infrastructure is both powerful and reliable. ■

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LAA Attenuator Arrays Save Space, Power and Time

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The programmable variable attenuator is a standard piece of hardware in RF labs. It controls RF signal levels for various kinds of testing. Multi-channel attenuation arrays can facilitate handovers between radio sources. A typical RF lab will have many of these devices. They can take up a lot of space and use a lot of power.

The Compact LAA series of attenuators from Acentury solves these problems. These digital attenuators have all the features and capabilities of a regular, full-size multi-channel variable attenuator but in a much smaller form factor. They take up much less space on a test station desk and can even fit inside a small desktop RF shield box. ***Figure 1*** shows an example of one of the attenuators in the Compact LLA series of attenuators.

Fig. 1 LAA8 Compact 8-channel attenuation array.

The family contains four-, six-, eight- and 16-channel versions with impressive performance specifications. Supporting a frequency range of 500 MHz to 7.5 GHz, the LAA Compact series of attenuators offer 0 to 95 dB of variable attenuation up to 6 GHz and 0 to 80 dB of attenuation from 6.0 to 7.5 GHz. The least significant attenuation bit value for all family members is 0.25 dB for both frequency ranges. With a maximum input power of +30 dBm and channel-to-channel isolation greater than 80 dB, these units are perfect for nearly any type of RF testing. The Compact LAA series is powered directly with 5 VDC or via USB-C. Using an adapter, these attenuators can also be powered via Power over Ethernet (PoE), providing significant flexibility in the lab. ***Figure 2*** shows the LAA4 Compact 4-channel attenuation array in a typical application.

Table 1 shows the performance of the attenuator family. While all members of the family achieve the same performance specifications, the 4-channel version is quite compact, measuring 130 × 67 × 21 mm in size. The 16-channel version, the largest of the Compact LAA series, is only 370 × 67 × 21 mm. This is less than 3x the size of the 4-channel model, with 4x the capacity. The Compact LAA series uses SMA connectors to achieve this size reduction and has no external display. Therefore, fewer internal electronics are required, which results in lower power consumption.

Fig. 2 **LAA4 Compact 4-channel attenuation array inside an RF shield box.**

TABLE 1

COMPACT LAA SERIES PERFORMANCE SPECIFICATIONS

Attenuator Family Specifications				
Frequency range	0.5 to 7.5 GHz			
Impedance	50 Ohms			
VSWR	1.5:1 typical, 2.0:1 maximum			
Insertion loss	< 16 dB			
Attenuation range	0 to 95 dB/0.25 dB step at 0.5 to 6 GHz 0 to 80 dB/0.25 dB step at 6 to 7.5 GHz			
Channel-to-channel isolation (0 dB attenuation for all channels)	> 80 dB			
Attenuation accuracy	(±0.3 + 6% attenuation setting) dB typical			
RF input power	30 dBm			
Switching speed	2 µs typical			
RF connector	SMA female			
Operating temperature	-20°C to +70°C			
Power supply	DC power supply: +5 VDC AC power supply: 100 to 240 VAC at 47 to 63 Hz			
DC power supply interface	DC005-5.5x2.1 USB (Type-C)			
Remote control	LAMTA control software via Ethernet (RJ45), USB-C			
Model number	LAA4	LAA6	LAA8	LAA16
Dimensions (L x W x H mm)	130 x 67 x 21	170 x 67 x 21	210 x 67 x 21	370 x 67 x 21

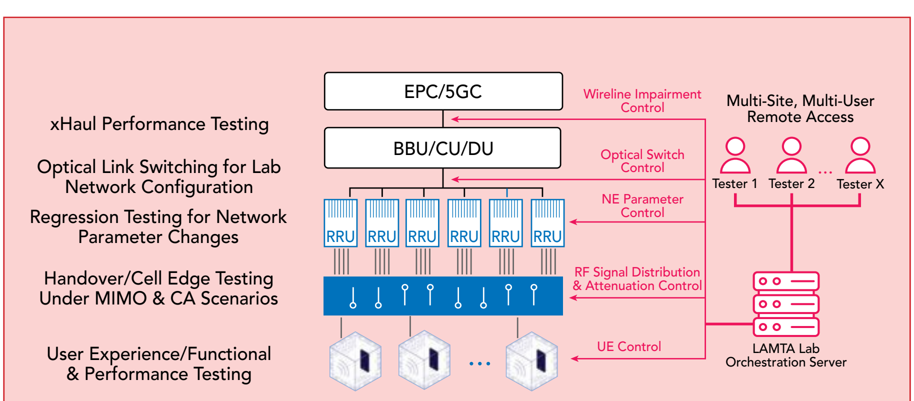

Fig. 3 **LAMTA lab orchestration block diagram.**

REMOTE ATTENUATION CONTROL VIA LAMTA SOFTWARE

Without a display or local control interface, the Compact LAA series attenuators are controlled via LAMTA software. LAMTA is an RF lab orchestration platform that provides RF signal distribution and attenuation control. Through a local or Ethernet connection, LAMTA controls the attenuation levels on each channel of the Compact LAA independently to facilitate handovers and other capabilities.

In addition to controlling Compact LAA series attenuators, LAMTA can also control RF attenuation matrices and switches for RF distribution control. This control and these devices allow RF resources to be shared among multiple test stations and locations. LAMTA also supports attenuation equipment from other manufacturers, such as Quintech, octoScope, Mini-Circuits and more. Beyond RF signal distribution and attenuation control, LAMTA also controls other lab equipment to orchestrate end-to-end testing. There are options to control Android UE, network elements via TR.069 and optical link impairment using the Xena Chimera. ***Figure 3*** shows the LAMTA platform block diagram.

LAMTA can control a single attenuator or an entire lab full of equipment using a browser-based GUI from a remote location. It can save hours of manual test setup and tear-down efforts that require physical, on-site presence. With LAMTA, the lab can be reconfigured in minutes to run different tests. Once the test is ready, LAMTA can replicate complex RF scenarios such as handovers under MIMO and carrier aggregation.

Acentury's RF lab solution provides an ideal combination for lab managers: compact LAA Series attenuators that save space and power and LAMTA software that helps save testing time and labor costs while enabling more sophisticated testing scenarios.

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Richmond Hill, Ontario
acentury.co

Polyrod Antenna Fits Many Applications

IERUS Technologies presents its latest wideband polyrod antenna innovation, setting a new standard for high gain and polarization purity in advanced applications. These antennas are crafted precisely using cutting-edge simulation technology from Nullspace EM and unique RF manufacturing expertise from Fortify. They are engineered to excel in demanding scenarios such as mmWave communications, sensing, far-field test ranges, near-field scanning and material measurements.

The hallmark of the IERUS polyrod antennas lies in their performance and durability. Integrated with a state-of-the-art radome, these antennas offer enhanced environmental protection without compromising on RF performance. Our latest offering provides 10 to 17 dBi gain over 7 to 18 GHz, along with cross-polarization isolation exceeding 30 dB and a VSWR of less than 2:1. With a compact cross-section of less than 1.5 in. x 1.5 in., these polyrod antennas are ideal for applications requiring space-saving solutions.

IERUS is committed to providing tailored solutions for every need. For those seeking bespoke designs, IERUS offers customization services, leveraging our partnerships with Nullspace and Fortify to deliver solutions quickly and efficiently. Headquartered in Huntsville, Ala., IERUS Technologies is a leader in electromagnetic hardware and software research, development and production. With a focus on providing high-value solutions to the most challenging problems of our customers, our collaborative approach across the IERUS, Fortify and Nullspace teams enables us to address unique customer challenges swiftly and effectively, unlocking advanced solutions that were once deemed unattainable.

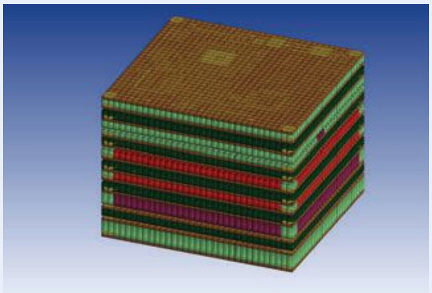
Experience the future of antenna technology with IERUS Technologies' polyrod antennas, where innovation meets performance and possibilities are limitless.

IERUS Technologies
Huntsville, Ala.
www.ierustech.com

Fortify
Boston, Mass.
https://3dfortify.com

Nullspace, Inc.
Irvine, Calif.
www.nullspaceinc.com

Gauss Stack Solves PCB Reliability Issues



Avishtech's Gauss Stack provides industry-leading stack-up design and transmission line signal integrity capabilities. It also enables users to simulate and address critical printed circuit board (PCB) reliability failure modes, including board and package-level warpage, reliability issues in plated through holes and solder joints and resin starvation and delamination risks. Gauss Stack also allows users to simulate the reliability of microvias through reflow, thermal cycling testing, service life and/or any set of thermal excursions.

This capability has become critically important with emerging requirements for high-density interconnect boards. The rapid simulations, coupled with the fully integrated materials library, allow users to assess the reliability of a given stack-up and rapidly make modifications and iterate through to an optimal solution without needing to build and test prototype boards. This can substantially decrease the time and cost required for a development cycle.

In the latest version of Gauss Stack Pro, the enhanced version of Gauss Stack that extends these capabilities to the layout, users can perform advanced simulations that couple local, layout-specific, dielectric variations within each layer with delamination risks and microvia reliability.

All the results generated by Gauss Stack and Gauss Stack Pro have undergone rigorous validation and demonstrate excellent agreement with real-world measurements. This level of accuracy allows users to precisely evaluate reliability risks right at the design stage, fostering a sense of trust and confidence in the software.

Avishtech serves the PCB industry with design and simulation software. Learn how Gauss Stack, Gauss Stack Pro and Avishtech's other Gauss offerings can help you computationally prototype your PCBs.

Avishtech
San Jose, Calif.
www.avishtech.com

European Microwave Week 2024

The only European event dedicated to the Microwave and RF industry

The European Microwave Week 2024 takes place in the vibrant city of Paris. Bringing industry and academia together, the European Microwave Week 2024 is a SIX day event, including THREE cutting edge conferences, THREE Forums and ONE exciting trade and technology Exhibition featuring leading players from across the globe. EuMW 2024 provides access to the very latest products, research and initiatives in the microwave sector. It also offers you the opportunity for face-to-face interaction with those driving the future of microwave technology. EuMW 2024 will see an estimated 1,600 conference delegates, over 4,000 attendees and in excess of 300 international exhibitors (inc. Asia & US).

The Exhibition

Registration to the exhibition is FREE!

- Over 300 International Companies - meet the industry's biggest names and network on a global scale
- Cutting-edge Technology - exhibitors showcase their latest product innovations, offer hands-on demonstrations and provide the opportunity to talk technical with the experts
- Industrial Workshops - get first hand technical advice and guidance from some of the industry's leading innovators

Entry to the exhibition is FREE.
Register at: www.eumweek.com

Be There

Exhibition Dates	Opening Times
Tuesday 24 September 2024	09:30 - 18:00
Wednesday 25 September 2024	09:30 - 17:30
Thursday 26 September 2024	09:30 - 16:30

The Conferences

The EuMW 2024 consists of three conferences, three forums and associated workshops:

- European Microwave Integrated Circuits Conference (EuMIC) 23 -24 September 2024
- European Microwave Conference (EuMC) 24 -26 September 2024
- European Radar Conference (EuRAD) 25 - 27 September 2024
- Plus Workshops and Short Courses (From 22 September 2024)
- In addition, EuMW 2024 will include the Defence, Security and Space Forum, the Automotive Forum and the 6G Forum

The three conferences specifically target ground breaking innovation in microwave research. The presentations cover the latest trends in the field, driven by industry roadmaps. The result is three superb conferences created from the very best papers submitted. For the full and up to date conference programme including a detailed description of the conferences, workshops and short courses, please visit www.eumweek.com. There you will also find details of our partner programme and other social events during the week.

TO SEE THE CONFERENCE SESSION MATRIX please visit: www.eumweek.com/docs/2024_programme_matrix.pdf

How to Register

Registering as a Conference Delegate or Exhibition Visitor couldn't be easier. Register online and print out your badge in seconds onsite at the Fast Track Check In Desk. Online registration is open now, up to and during the event until 27 September 2024.

- Register online at **www.eumweek.com**
- Receive an email receipt with QR code attached
- Bring your email, QR code and photo ID with you to the event
- Go to the Fast Track Check In Desk and print out your badge
- Alternatively, you can register onsite at the self service terminals during the registration.

Please note: NO badges will be mailed out prior to the event.

On-site registration opening times:

- Saturday 21 September 2024 (16:00 - 19:00)
- Sunday 22 - Thursday 26 September 2024 (08:00 - 17:00)
- Friday 27 September 2024 (08:00 - 10.00)

Registration Fees

Full Week ticket:

Get the most out of this year's Microwave Week with a Full Week ticket. Combine all three conferences with access to the Defence, Security and Space Forum and the 6G Forum (the Automotive Forum and the Schools are not included) as well as all the Workshops or Short Courses.

Registration at one conference does not allow access to the sessions of the other conferences.

Reduced rates are offered if you have society membership to any of the following: EuMA, GAAS, IET or IEEE. Reduced rates for the conferences are also offered if you are a Student/Senior (Full-time students 30 years or younger and Seniors 65 or older as of 27 September 2024). The fees shown below are invoiced in the name and on behalf of the European Microwave Association. All payments must be in € Euros – cards will be debited in € Euros.

ALL FEES ARE INCLUSIVE OF FRENCH VAT @ 10%.

New for 2024! Lunches are included with all conference/forum and workshop registrations:

– Sunday: lunch boxes provided to delegates

– Monday–Friday: delegates receive a seated 3 course lunch

CONFERENCES REGISTRATION	ADVANCE DISCOUNTED RATE (FROM NOW UP TO & INCLUDING 23 August 2024)				STANDARD RATE (FROM 24 August 2024 & ONSITE)			
	Society Member		Non-Member		Society Member		Non-Member	
1 Conference	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.
EuMC	€ 630	€ 180	€ 880	€ 250	€ 880	€ 250	€ 1,230	€ 350
EuMIC	€ 480	€ 160	€ 670	€ 220	€ 670	€ 220	€ 940	€ 310
EuRAD	€ 430	€ 150	€ 600	€ 200	€ 600	€ 200	€ 830	€ 290
2 Conferences	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.
EuMC + EuMIC	€ 890	€ 340	€ 1,240	€ 470	€ 1,240	€ 470	€ 1,740	€ 660
EuMC + EuRAD	€ 840	€ 320	€ 1,180	€ 450	€ 1,180	€ 450	€ 1,650	€ 640
EuMIC + EuRAD	€ 730	€ 300	€ 1,020	€ 420	€ 1,020	€ 420	€ 1,420	€ 590
3 Conferences	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.
EuMC + EuMIC + EuRAD	€ 1,070	€ 480	€ 1,500	€ 670	€ 1,500	€ 670	€ 2,110	€ 940
Full Week Ticket	€ 1,550	€ 910	€ 2,100	€ 1,190	€ 2,100	€ 1,190	€ 2,840	€ 1,590

BECOME A MEMBER - **NOW!**

EuMA membership fees: Professional € 25 / year, Student € 15 / year.

One can apply for EuMA membership by ticking the appropriate box during registration for EuMW. Membership is valid for one year, starting when the subscription is completed. The discount for the EuMW fees applies immediately. Members have full e-access to the International Journal of Microwave and Wireless Technologies.

EUMA KNOWLEDGE CENTRE

The EuMA website has its Knowledge Centre which presently contains over 24,000 papers published under the EuMA umbrella. Full texts are available to EuMA members only, who can make as many copies as they wish, at no extra-cost.

SPECIAL FORUMS AND SESSIONS REGISTRATION		ADVANCE DISCOUNTED RATE (UP TO & INCLUDING 23 August 2024)		STANDARD RATE (FROM 24 August 2024 & ONSITE)	
	Date	Delegates*	All Others**	Delegates*	All Others**
Automotive Forum	23 September 2024	€ 325	€ 455	€ 455	€ 635
Defence, Security & Space Forum	25 September 2024	€ 70	€ 100	€ 100	€ 140
6G Forum	26 September 2024	€ 70	€ 100	€ 100	€ 140
Design School	24 September 2024	€ 40	€ 55	€ 40	€ 55
Radar School	26/27 September 2024	€ 40	€ 55	€ 40	€ 55
Gala Dinner	25 September 2024	€ 60	€ 60	€ 60	€ 60

*those registered for EuMC, EuMIC or EuRAD **those not registered for a conference

Workshops and Short Courses

Despite the organiser's best efforts to ensure the availability of all listed workshops and short courses, the list below may be subject to change. Also workshop numbering is subject to change. Please refer to www.eumweek.com at the time of registration for final workshop availability and numbering.

Sunday 22 September 2024			
WS-01		Full Day	Terahertz technologies, millimeter-waves, circuits and system implementations of devices
WS-02		Full Day	Key Enabling Technologies for Future Wireless, Wired & Satcom Applications
WS-03		Full Day	Challenges and design considerations for characterizing sub-THz and 6G communication links
WS-04		Full Day	Disruptive sub-THz antenna and transceiver systems for future sensing, localization and communication
WS-05		Full Day	Technologies and Circuits for 5G RF Front End Modules and Evolution to 6G
WS-06		Half Day	Comprehensive Exploration of GaN Device and Power Amplifier (PA) Technologies: From Fundamentals to the Latest Applications in 5G and Beyond.
WS-07		Full Day	Design, characterization, and integration challenges in active phased arrays for wireless communications
WS-08		Full Day	Photonic Technologies for Radio Frequency Applications
WS-09		Half Day	Towards THz communication: implementation and propagation challenges in harsh environments
WS-10		Half Day	Ultra-wideband efficient PAs and broadband matching design techniques
SC-01		Full Day	Fundamentals of PA design
WS-11		Half Day	Recent Advances in Topologies, Technologies and Practical Realizations of Microwave Sensors
WS-12		Half Day	Reconfigurable devices using new materials and technologies
WS-13		Half Day	RF and Microwave Systems for Edge Intelligence
WS-14		Half Day	Characterization, Calibration, and Production Test of Phased Array Antennas (PAA) for Non-Terrestrial-Network (NTN)

Monday 23 September 2024			
WM-01		Full Day	Space (Sub)millimetre-wave Receivers for Earth Observation and Planetary Science
WM-02		Full Day	On-wafer measurements and material characterisation for communications and quantum applications
WM-03		Half Day	Last advances in scanning microwave microscopy including metrology and emerging applications
WM-04		Half Day	Packaging and RFICs for Wireless Communication and Radar Sensing above 100 GHz

Thursday 26 September 2024			
WTh-01		Half Day	Integrated Microwave Photonics for communication and sensing
WTh-02		Half Day	Radar Networks
WTh-03		Half Day	Integrated antenna systems for next-generation D-band communication and radar systems
WTh-04		Full Day	Microwave Photonics for Wireless Sensing
SC-03		Full Day	Basics of Systems Engineering for the Microwave Engineering Community

Friday 27 September 2024			
WF-01		Full Day	Last advances in free-space radar sensing for electromagnetic materials modelling and characterization
WF-02		Full Day	Chipless RFID Systems: Future and Challenges
SC-02		Half Day	Introduction to implantable antennas: implant antenna design methodology, numerical analysis and modelling, prototyping and testing, and phantoms
SC-04		Half Day	Radar Waveform Optimization Mastery
WF-03		Full Day	Advanced SAR processing techniques for security and safety applications

WORKSHOPS AND SHORT COURSES	IN COMBINATION WITH CONFERENCE REGISTRATION				WITHOUT CONFERENCE REGISTRATION			
	Society Member		Non-Member		Society Member		Non-Member	
	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.	Standard	Student/Sr.
Half Day	€ 120	€ 90	€ 160	€ 120	€ 160	€ 120	€ 210	€ 160
Full Day	€ 170	€ 130	€ 230	€ 170	€ 230	€ 170	€ 300	€ 230

Spectrum Clearing and Geo-Locating Legacy Signals

Anritsu's app note details how to perform a spectrum clearing sweep and signal geo-location with the Mobile Interference Hunter MX280007A system and FieldMasterPro MS2090A.

Anritsu

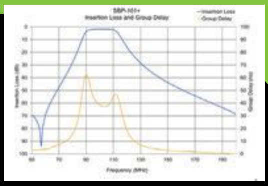
https://bit.ly/45dih1s

Group Delay in RF Filters

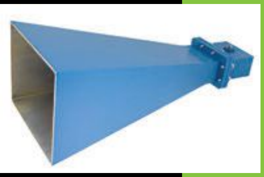
Understand group delay in this brief application note, which examines phase delay and group delay, plus illustrations and a display of magnitude and group delay frequency response curves for two real filters.

Mini-Circuits

https://blog.minicircuits.com/rf-group-delay/



Differences Between Directional and Omnidirectional Antennas



Check out this Pasternack blog to learn the key differences between directional and omnidirectional antennas and their unique applications.

Pasternack

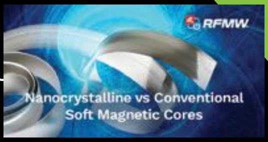
https://bit.ly/4c5Athj

Nanocrystalline vs. Conventional Soft Magnetic Cores

Soft magnetic cores play a crucial role in RF applications. Traditionally, materials like silicon steel, ferrite and amorphous cores have dominated the solutions available. However, a promising alternative has emerged in the form of nanocrystalline cores, versus these conventional soft magnetic cores, offering a paradigm shift in performance and efficiency.

RFMW

https://bit.ly/3yKbdit



Pickering Interfaces Celebrates 25 Years in PXI

In 2024, Pickering Interfaces, the leading provider of modular signal switching and sensor simulation products for electronic test and verification, is celebrating 25 years of supporting PCI eXtensions for Instrumentation (PXI), the scalable, high performance modular instrumentation standard first introduced in 1997.

Pickering Interfaces

www.pickeringtest.com

BB60C Spectrum Analyzer: Your Key to EMC Success

In this in-depth exploration of the BB60C, Sean R. Phillips and Justin Crooks from Signal Hound delve into the intricacies of EMC pre-compliance testing, highlighting how this powerful device can revolutionize your approach to signal analysis and interference hunting.

Signal Hound

www.youtube.com/watch?v=DbDz2HLwSkw

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DEVICES/COMPONENTS/MODULES

Embedded Filtering for X-Band Deployable Satcoms

A1 Microwave have combined their waveguide components and microwave filtering expertise to offer complete custom-designed embedded filtering solutions. These are especially suitable for deployable 'manpack' applications where dense packaging of the waveguide components is essential, along with improved performance and reliability as well as reduced weight.

A1 Microwave
www.a1microwave.com

Wideband Multichannel RF Digitizers

VENDORVIEW

Analog Devices' ADSY1100-series is a family of wideband multichannel RF digitizers in a 3UVPX SOSA™-aligned format. The system is built around ADI's next-generation "Apollo" MXFE™ product (AD9084) featuring DAC sample rates up to 28 GSPS and ADC sample rates up to 20 GSPS in a 4 Tx/4 Rx configuration. ADSY1100's integrated digital signal processing reduces system power consumption, while the integrated RF tuner reduces end system size and complexity.

Analog Devices
www.analog.com

High-Power RF Terminations

VENDORVIEW

Fairview Microwave announced the launch of its high-power RF terminations. They are designed to enhance signal integrity in demanding applications across telecommunications, aerospace and defense sectors. The newly unveiled terminations feature cutting-edge 4.3-10, 7/16 DIN and N-type connectorized designs, supporting a maximum frequency range up to 6 GHz and power levels up to 50 W, setting a standard for reliability and performance.

Fairview Microwave
www.fairviewmicrowave.com

Mechanical Switch

VENDORVIEW

Mini-Circuits' model ZK-MSP2TA-18 is a single-pole, double-throw electro-mechanical switch with TTL-controlled operation from DC to 18 GHz. Typical insertion loss is 0.3 dB while isolation between ports is 66 dB or better across the full bandwidth. The operating lifetime is typically 5 million switching cycles with a typical switching time of 25 ms. Suitable for radar, radio and test applications, the absorptive, 50 Ω failsafe switch includes an LED switch state indicator and is fitted with SMA female coaxial connectors.

Mini-Circuits
www.minicircuits.com

Highpass Filter

VENDORVIEW

Quantic PMI Model HP8G-7D8G-CD-SMF is a highpass filter with a passband of 8 to 22 GHz. The compact 1.15 × 0.70 × 0.50 in. housing is outfitted with SMA connectors (male input, female output) and is silver plated to provide the highest possible Q. Other specifications include 3 dB cutoff of 7.6 GHz; input power 5 W typical, 10 W maximum; ripple 0.35 dB; passband VSWR: 2.0:1; and -35 dB typical at 7.5 GHz rejection.

Quantic PMI
www.quanticpmi.com

GaAs Passive MMIC Balun

VENDORVIEW

The Marki Microwave MBAL-0220CSP2 is a GaAs passive MMIC balun featuring a frequency range of 2 to 20 GHz and is tuned for optimal 0.3 dB amplitude and 3 degrees phase balance across the entire band. It is an ideal solution to interface into data converters for S-K-Band digital beamforming and other higher order Nyquist sampling applications, clock distribution and balanced amplifiers.

RFMW
www.rfmw.com

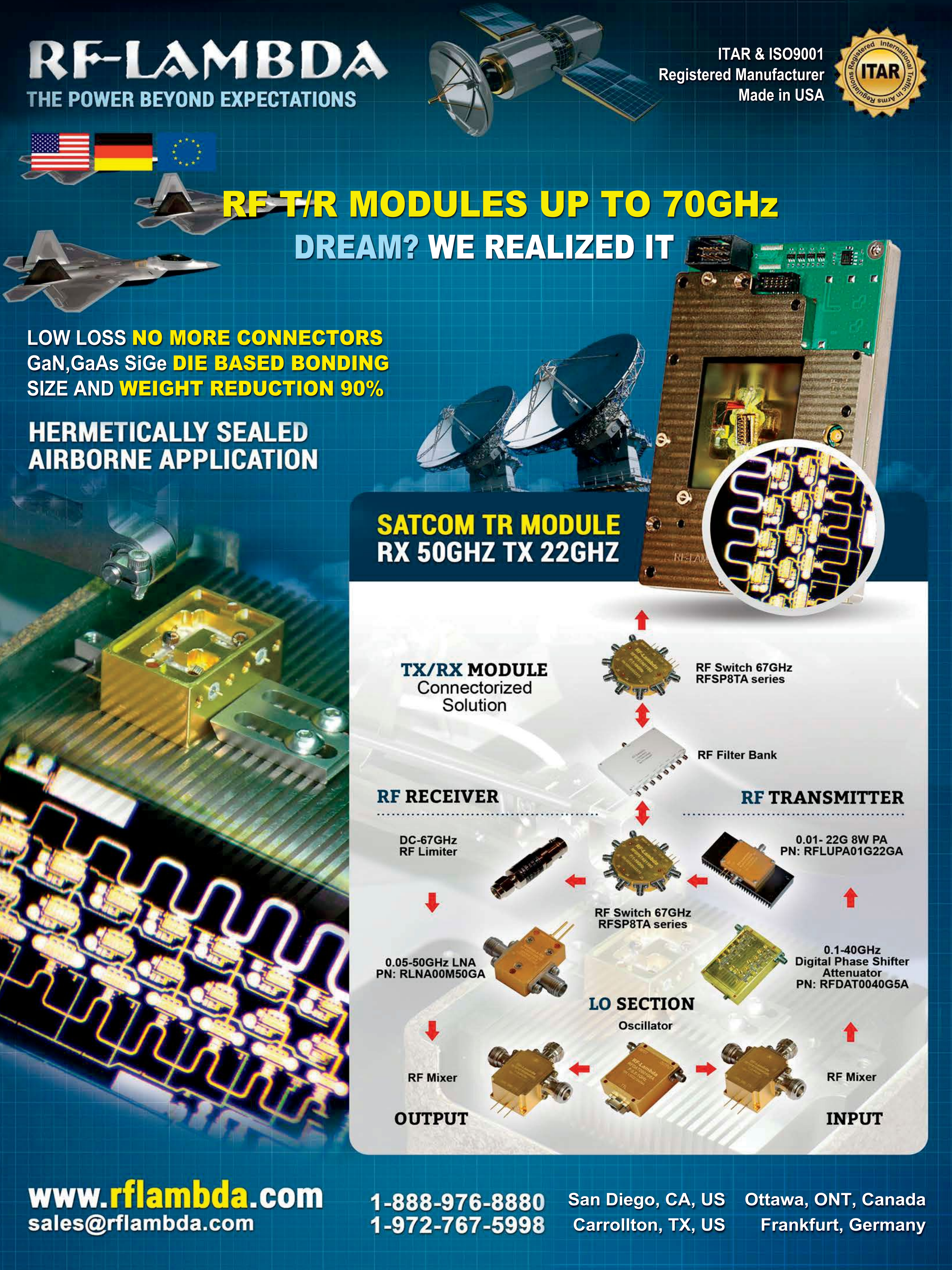
ANTENNAS

mmWave Horn Antennas

VENDORVIEW

Pasternack launched its new series of mmWave horn antennas. Designed to meet the evolving needs of test and measurement applications in the fast-paced tech industry, the new line includes a variety of waveguide probe antennas and dual polarized horn antennas, offering enhanced flexibility and performance in the 22 to 170 GHz frequency range.

Pasternack
www.pasternack.com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HERMETICALLY SEALED
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RF TRANSMITTER
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Review by: Katerina Galitskaya

Bookend

Planar Microwave Sensors

Paris Vélez, Lijuan Su, Jonathan Muñoz-Enano and Ferran Martín

Planar Microwave Sensors written through the collaboration of four experts in the field of microwave engineering, has a clear way of explaining the principles, design and applications of planar microwave sensors. The book begins with an overview of microwave sensing technologies, comparing planar sensors with other sensing methods and giving a good understanding of modern sensor solutions. Moving forward, the reader gets familiar with specific sensing mechanisms, starting with frequency-variation sensors, which are crucial for the dielectric characterization of materials and have potential applications in healthcare. The authors go into phase variation sensors next, offering insights into sensitivity optimization techniques and possible applications, including motion sensing. Next is the topic of coupling-modulation sensors, which is particularly relevant for motion control in industrial scenarios and material characterization. The book provides a comprehensive overview of frequency-splitting sensors, highlighting their robustness against ambient factors and methods to enhance sensitivity and differential-mode sensors, emphasizing their high sensitivity and resolution, especially in applications like electrolyte concentration detection in biological samples. Lastly, the authors address an interesting topic of RFID sensors, discussing both chipped and chipless varieties and their applications across various fields. *Planar Microwave Sensors* is a valuable resource for engineers, students and researchers in sensing technologies, RF engineering, IoT systems and related fields. The book provides comprehensive theoretical foundations, practical insights and experimental validations in a clear and understandable way. With its focus on planar microwave sensors and their wide-ranging applications, the authors bring great value to the RF community and contribute significantly to advancements in sensing and IoT technology in the future.

ISBN: 978-1-119-81103-9
Pages: 480

To order this book contact:
Wiley (September 2022)
wiley.com/en-us

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DC TO 110 GHz

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FABS and LABS

NHanced Semiconductors: Making the Impossible Possible




NHanced Semiconductors has its headquarters in Illinois, an R&D and prototyping fab in North Carolina and a recently opened advanced package assembly facility in Indiana. The company's evolution and growing importance in packaging and heterogeneous integration are a testament to its expertise. Founded in 2016 by current CEO and owner Bob Patti, NHanced Semiconductors emerged as a spin-out of Tezzaron Semiconductor, which evolved from ASIC Designs. ASIC Designs was an R&D company specializing in high performance systems and ASICs and was Bob Patti's first start-up endeavor. Tezzaron Semiconductor established itself as a leader in 3D-IC technology, developing its first working 3D ICs in 2004. The development lineage and expertise of NHanced Semiconductors have deep roots in these packaging and integration start-ups.

Since its inception, NHanced Semiconductors has been advancing and developing 2.5D/3D technologies, chiplet integration, smart interposers, die and wafer stacking and other advanced packaging techniques. The company prides itself on turning what they call "bleeding edge designs" into state-of-the-art 3D ICs and 2.5D assemblies. They call this manufacturing model "Foundry 2.0™."

The Foundry 2.0 concept is based on sourcing building blocks from high volume semiconductor foundries. NHanced combines these building blocks into different combinations using packaging technologies like through-silicon vias (TSVs), hybrid bonding and glass or silicon interposers. With this technique, the company works with state-of-the-art foundries as a third-party integrator to provide sophisticated, highly differentiated, heterogeneously integrated products to meet customer needs and requirements. NHanced Semiconductor takes pride in being the only U.S.-based foundry that can support this manufacturing model.

The Foundry 2.0 model has been a success. The NHanced footprint in its three current facilities is already well over 55,000 sq. ft., including 12,000 sq. ft. of Class 100 cleanroom. Rapid growth has been necessary to meet the market demand facing NHanced as the semiconductor industry increases its focus on innovation and specialty production.

The Foundry 2.0 model encompasses the entire process, from the original concept to full production. To accomplish this, the NHanced design team will support customers with project management, system-level designs, software development, hardware front-end designs, physical/back-end designs and support to get designs into prototyping and production. Once a design goes into the NHanced fab, the company takes care of all the necessary wafer processing, interconnection and manufacturing steps. From here, the devices go into packaging, assembly and test.

In these final steps, the company differentiates from most outsourced semiconductor assembly and test (OSAT) providers by serving customers needing low volume to medium volume complex device runs. In their production environment, NHanced targets engineering-heavy advanced package assemblies with extremely flexible manufacturing lines tuned for lower-volume production. Once the products are assembled, NHanced completes its end-to-end manufacturing cycle with in-house thermal cycling, HAST and probe testing. These capabilities are augmented by outside resources for a broad range of component testing and screening to ensure the highest yields for their end customers.

Utilizing this production model, NHanced targets opportunities in heterogeneous integration, additive silicon manufacturing, photonics, microfluidics and III-V compound semiconductors. These support large-scale electrification, 5G wireless communications and the widespread deployment of artificial intelligence in aerospace and defense, medical and industrial markets. The Foundry 2.0 model is helping NHanced Semiconductors make the impossible possible.

https://nhanced-semi.com/